

*16924 Woody/Buzz\_UMA KBL*  
*Schematics Document*

*DY : None Installed*  
*UMA: UMA only installed*  
*DIS: DISCRTE OPTIMUS installed*

Count		
<div>緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Cover Page		
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Main Func = CPU

eDP

55 eDP\_TX\_CPU\_N0 <<<  
55 eDP\_TX\_CPU\_P0 <<<  
55 eDP\_TX\_CPU\_N1 <<<  
55 eDP\_TX\_CPU\_P1 <<<

55 eDP\_AUX\_CPU\_N <<<  
55 eDP\_AUX\_CPU\_P <<<

55 eDP\_HPD\_CPU >>>  
24 eDP\_BLEN\_CPU >>>  
55 eDP\_BLCtrl\_CPU >>>  
55 eDP\_VDDEN\_CPU >>>

HDMI

57 HDMI\_DATA\_CPU\_N2 <<<  
57 HDMI\_DATA\_CPU\_P2 <<<  
57 HDMI\_DATA\_CPU\_N1 <<<  
57 HDMI\_DATA\_CPU\_P1 <<<  
57 HDMI\_DATA\_CPU\_N0 <<<  
57 HDMI\_DATA\_CPU\_P0 <<<  
57 HDMI\_DATA\_CPU\_N3 <<<  
57 HDMI\_DATA\_CPU\_P3 <<<

14,57 HDMI\_CLK\_CPU <<<  
14,57 HDMI\_DATA\_CPU <<<

57 HDMI\_DET\_CPU >>>

TYPEC

73 DP\_DDI\_TX\_N0 <<<  
73 DP\_DDI\_TX\_P0 <<<  
73 DP\_DDI\_TX\_N1 <<<  
73 DP\_DDI\_TX\_P1 <<<  
73 DP\_DDI\_TX\_N2 <<<  
73 DP\_DDI\_TX\_P2 <<<  
73 DP\_DDI\_TX\_N3 <<<  
73 DP\_DDI\_TX\_P3 <<<

73 DP\_AUX\_CPU\_N <<<  
73 DP\_AUX\_CPU\_P <<<

14 DDPC\_CTRLDATA <<<

73 DP\_HPD\_CON <<<

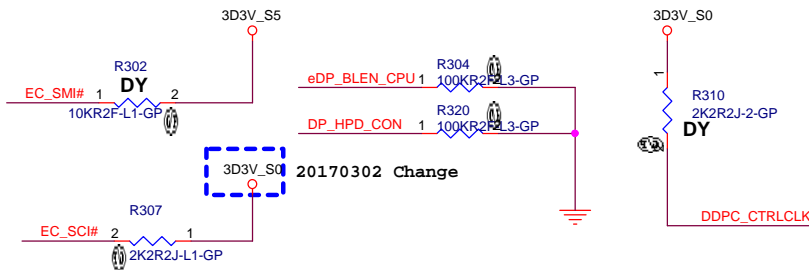
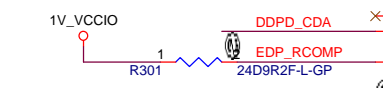
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14 DDPD\_CDA <<<  
24 EC\_SMI# >>>  
24 EC\_SCI# >>>

HDMI

TYPEC

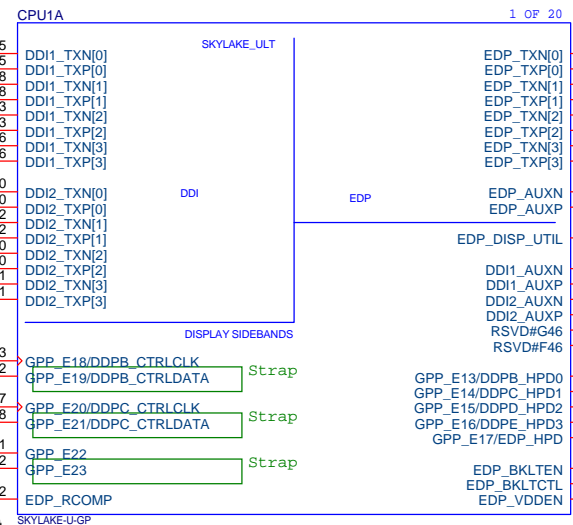
HDMI



(#543016) eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.



CPU

eDP

eDP

Count

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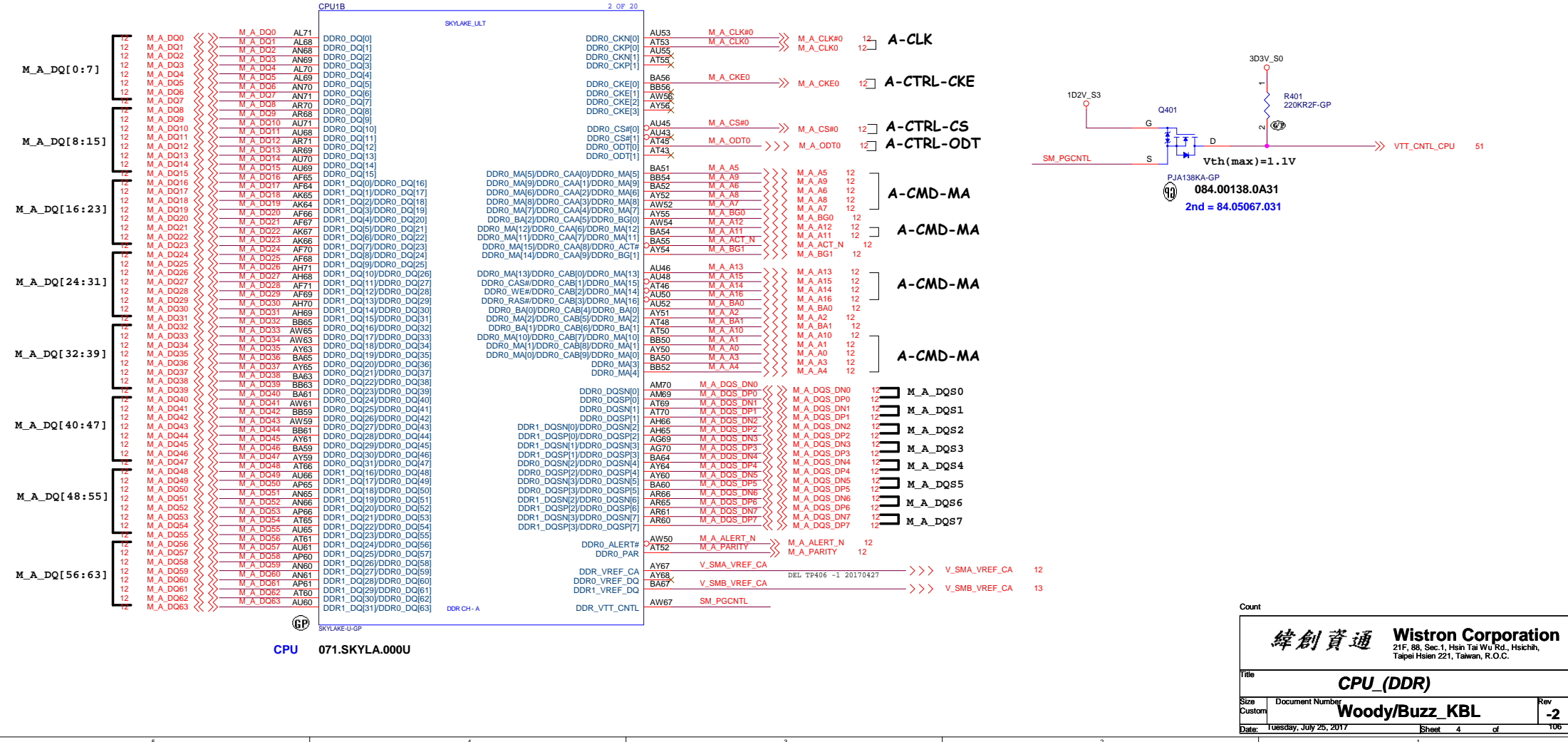
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Main Func = CPU

DDR4 ball type:NON Interleaved Type



Main Func = CPU

DDR4 ball type:NON Interleaved Type

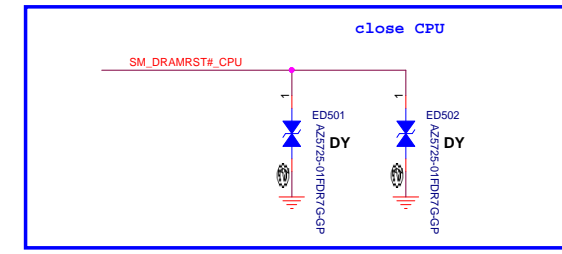
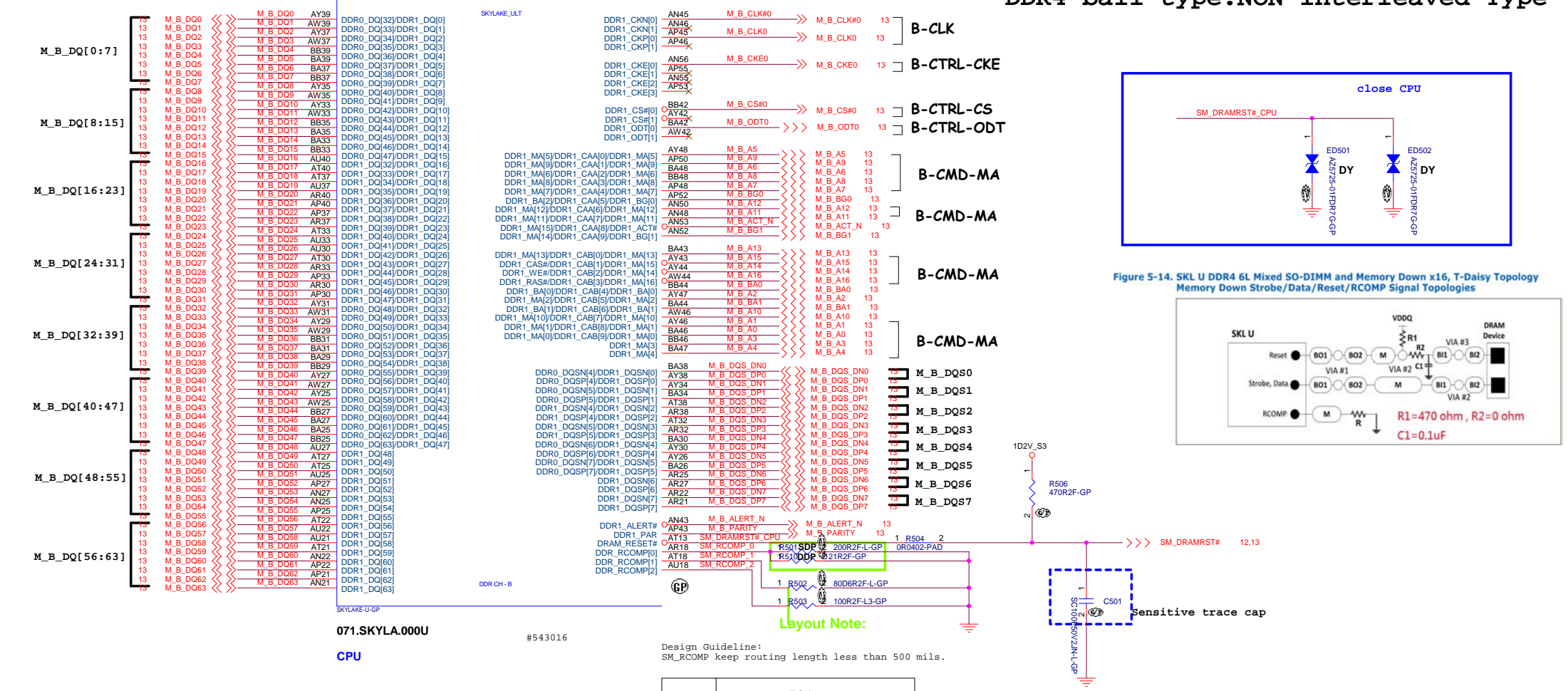
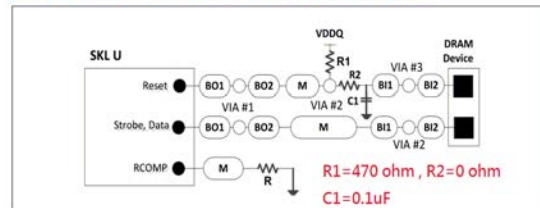


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



	R501
DDP	121ohm (64.12105.6DL)
SDP	200ohm (64.20005.6DL)

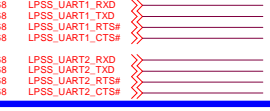
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Title CPU_(DDR)	
Size Custom	Document Number Woody/Buzz_KBL
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Main Func = PCH

DETECT&RESET



DEBUG PORT



I2C

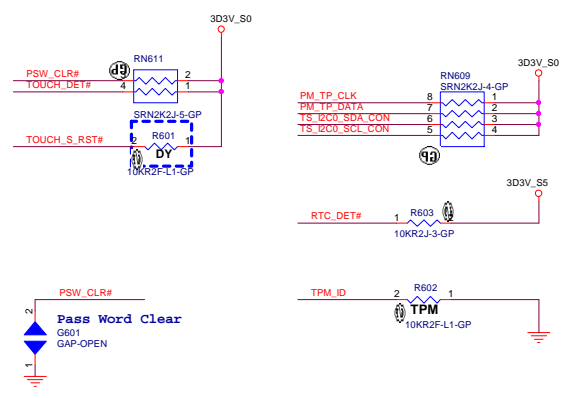


OTHER



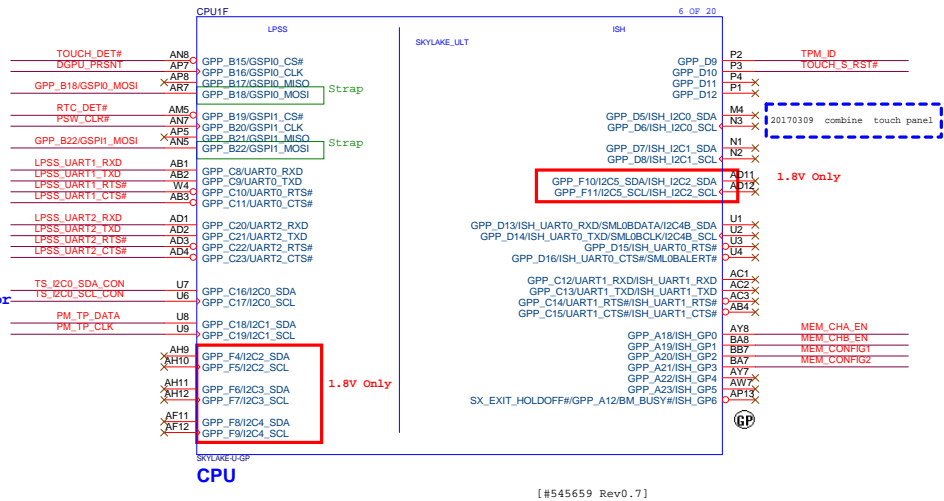
Touch Panel / G-Sensor

Touch Pad

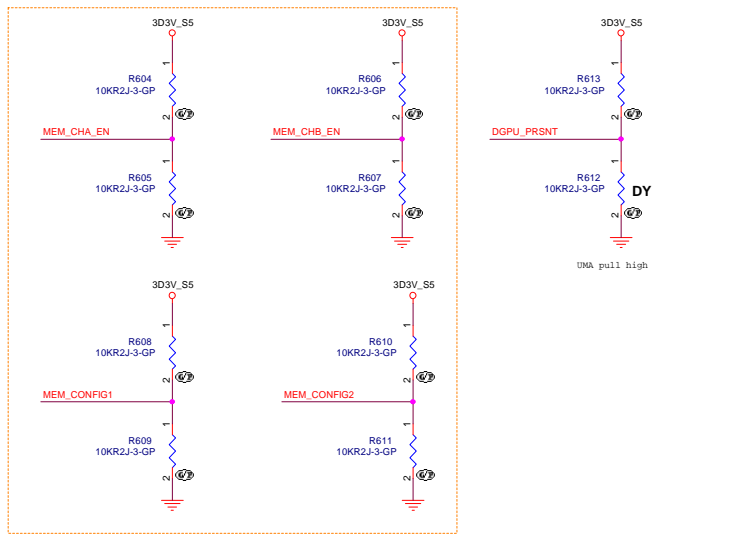


GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



[#545659 Rev0.7]



Vendor	GONFIG4 (GPP_A19)	CONFIG3 (GPP_A18)	CONFIG2 (GPP_A21)	CONFIG1 (GPP_A20)	Mfr.PN	Wistron PN	Capacity	DDP/SDP
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	KN.8GB0G.049	8Gb	SDP
MICRON	0	0	0	1	MT40A512M16JY-083E:B	KN.8GB04.013	8Gb	SDP
SAMSUNG	0	0	1	0	K4A8G165WB-BCRC	KN.8GB0B.048	8Gb	SDP
HYNIX	0	0	1	1	H5AN4G6NAFR-TF	KN.0040G.015	4Gb	SDP
HYNIX	0	1	0	0	H5AN4G6NAFR-UHC	KN.0040G.016	4Gb	SDP
MICRON	0	1	0	1	MT40A256M16GE-083E:B	KN.00404.010	4Gb	SDP
SAMSUNG	0	1	1	0	K4A4G165WE-BCRC	KN.0040B.014	4Gb	SDP
HYNIX	0	1	1	1	H5AN4G6N4FR-UHC	KN.0160G.010	16Gb	DDP
MICRON	1	0	0	0	MT40A1G16WBU-083E:B	KN.01604.001	16Gb	DDP

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Woody/Buzz\_KBL

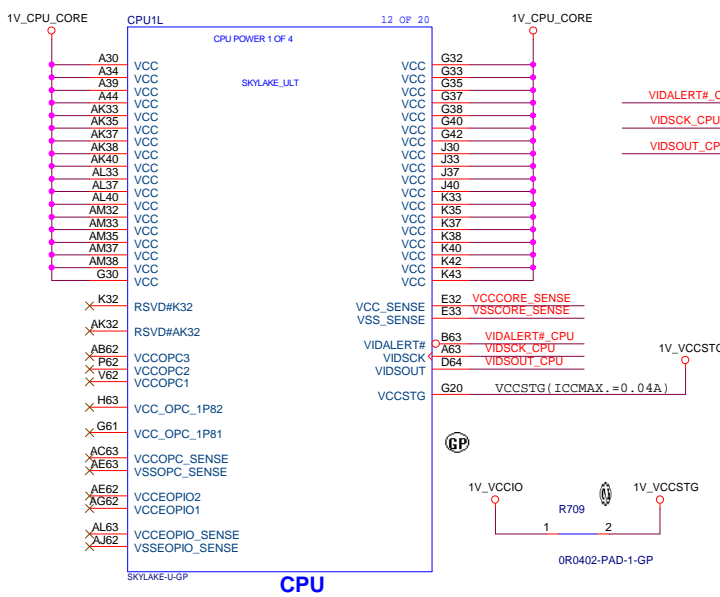
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Main Func = CPU

SVID

- 46 SVID\_ALERT#\_CPU <<< —
- 46 SVID\_CLK\_CPU <<< —
- 46 SVID\_DATA\_CPU <<< —
- 46 VCCCORE\_SENSE <<< —
- 46 VSSCORE\_SENSE <<< —



Layout Note:  
1. Place close to CPU  
2. VCC\_SENSE/ VSS\_SENSE  
impedance=50 ohm  
3. Length match<25mil

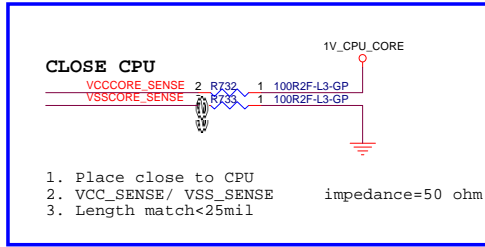
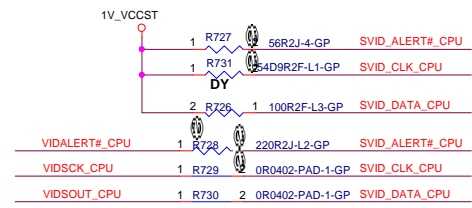


Figure 10-7. Routing Illustration for SVID Topology

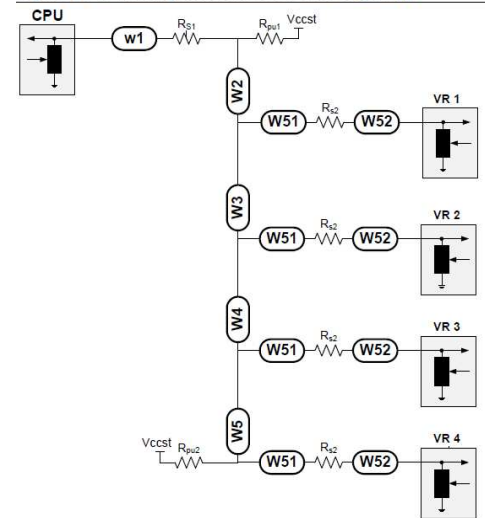


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>Pu1</sub> [Ω]	R <sub>Pu2</sub> [Ω]	R <sub>S1</sub> [Ω]	R <sub>S2</sub> [Ω]	VCC <sub>ST</sub> [V] <sup>T</sup>
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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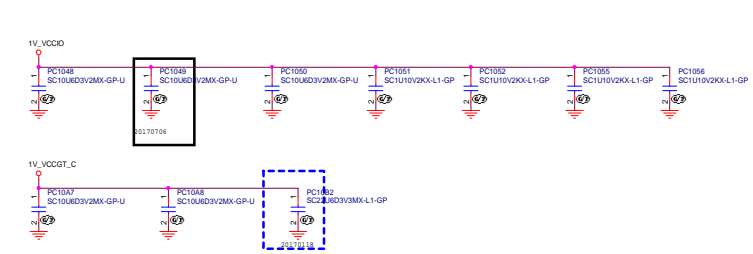
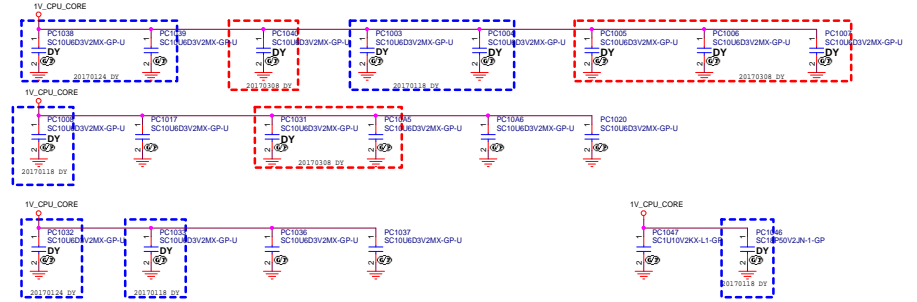
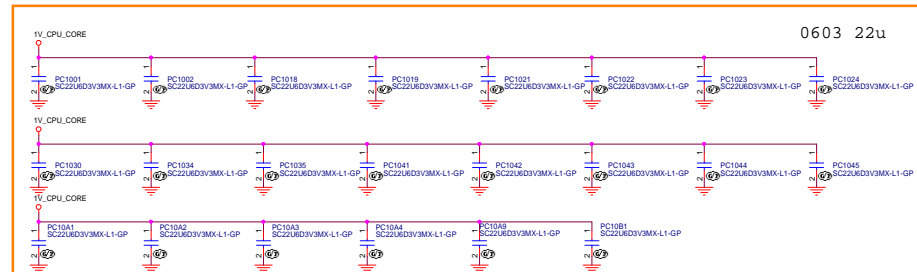


# Blanking

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### 48.1.3 Kaby Lake U Compatible Design Recommendation

#### 48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

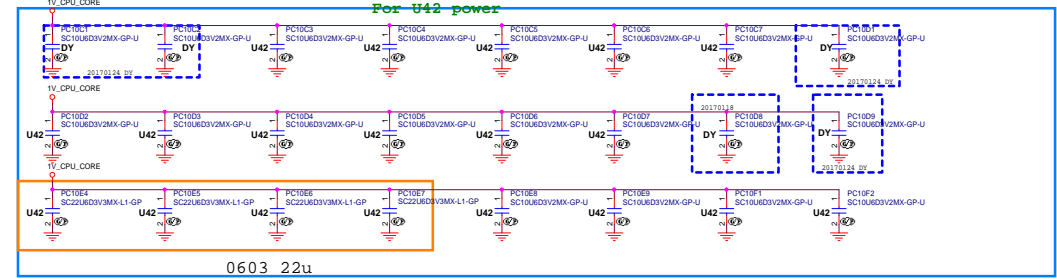
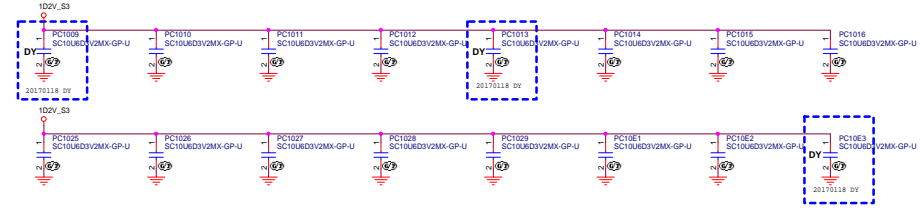
Bulk Decoupling Locations	Example - U +2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at primary side near to VR output
Vcc <sub>VR</sub> Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at backside side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output

Notes:  
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.  
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

### 1V\_CPU\_CORE

U22 0603 22uF \*22 , 0402 10uF\*11 , 1uF\*1

U42 0603 22uF \*4 , 0402 10uF\*15



1V\_VCCIO  
10uF \* 2 1uF \* 4

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)	
		8x 10 uF 0402	
Vcc/Vcc <sub>GT</sub>	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc <sub>GT</sub>	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)	

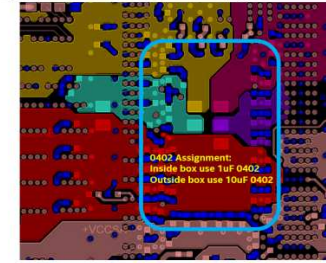
### 1D2V\_S3

0402 10uF\*13

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc <sub>S3</sub>	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
Vcc <sub>IO</sub>	6x 10 uF 0402		Place as close to the package as possible
Vcc <sub>Q</sub>	4x 1 uF 0402		Place as close to the package as possible
	4x 10 uF 0402		Place as close to the package as possible
	3 x 22 uF 0603		Place as close to the package as possible
V <sub>DDQ</sub>	1 x 10 uF 0402		Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example shown in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 4mm (RSC). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc <sub>LL</sub>	1x 1 uF 0402		Place as close to the package as possible.
Vcc <sub>LL_OC</sub>	1x 1 uF 0201		Do not route Vcc <sub>LL</sub> , Vcc <sub>LL_OC</sub> , Vcc <sub>Q</sub> closest adjacent layer over any power net other than ground.
Vcc <sub>ST</sub>	1x 1 uF 0402		For Vcc <sub>ST</sub> Refer to Figure 48-2 for additional routing details for Vcc <sub>ST</sub> & Vcc <sub>STG</sub> .

- Notes:  
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth: 250kHz e.g., 1MHz switching VR  
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps > Power source  
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.  
4. Diagram of placement for 0402 backside caps for CPU decoupling.



Count

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File CPU\_(Power CAP1)

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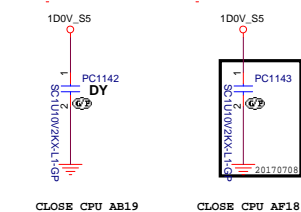
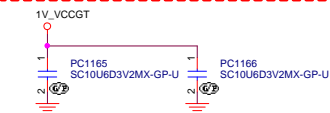
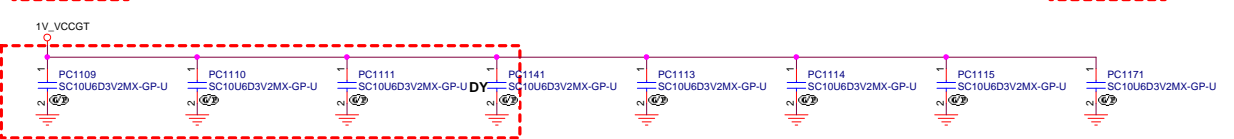
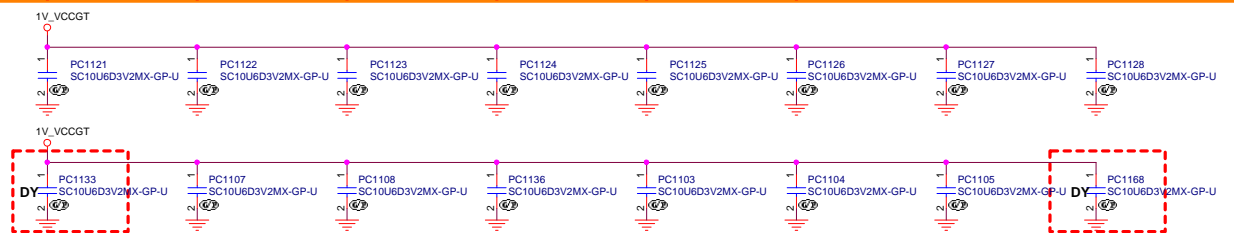
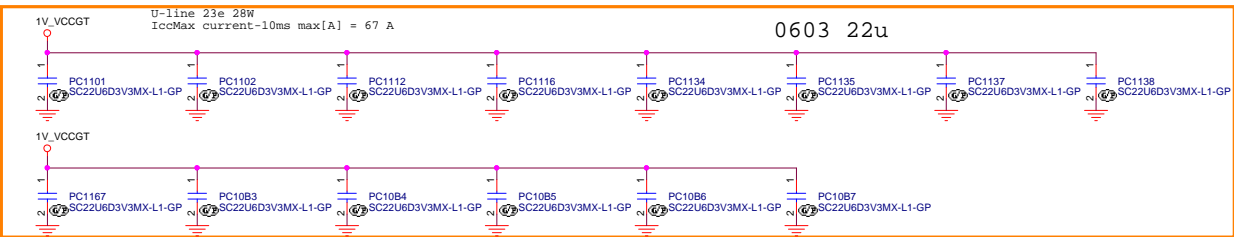
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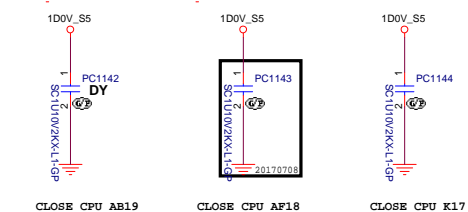
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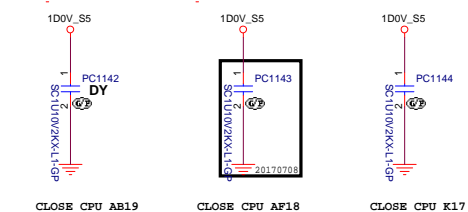
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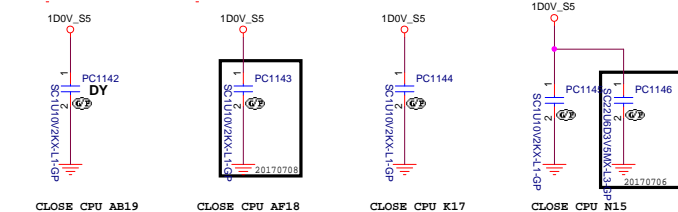
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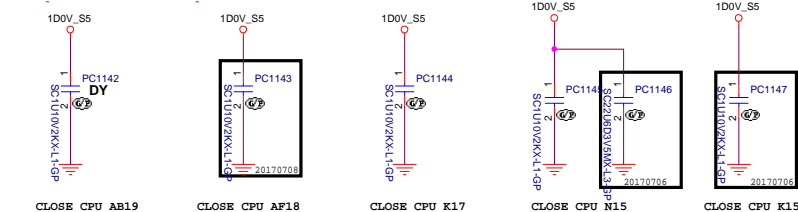
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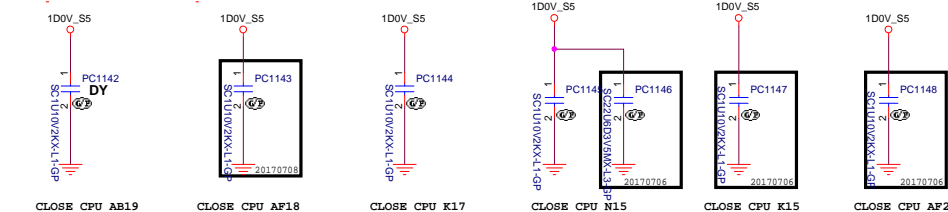
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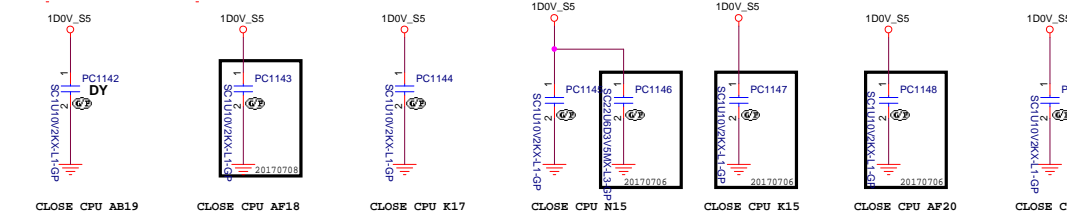
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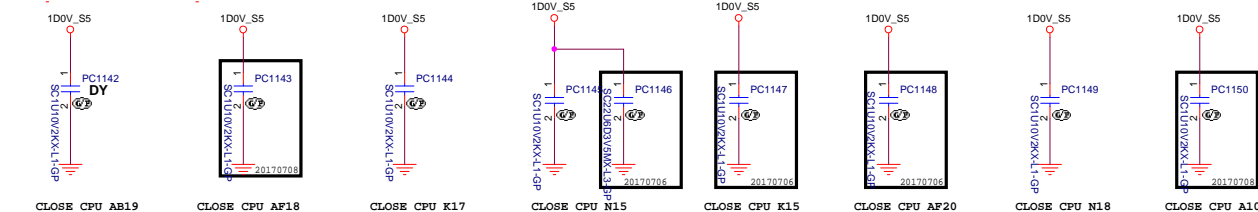
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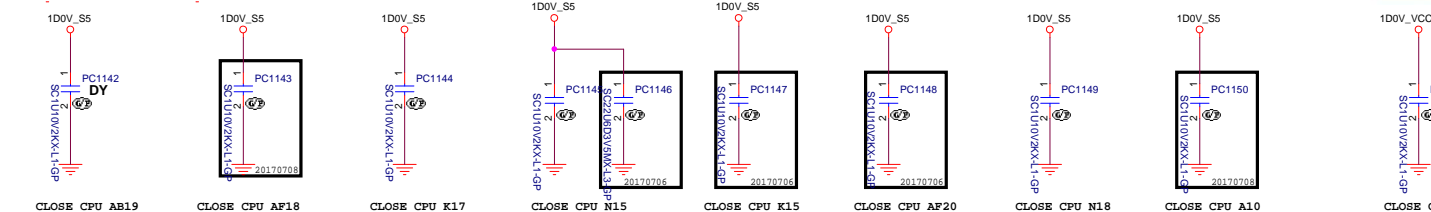
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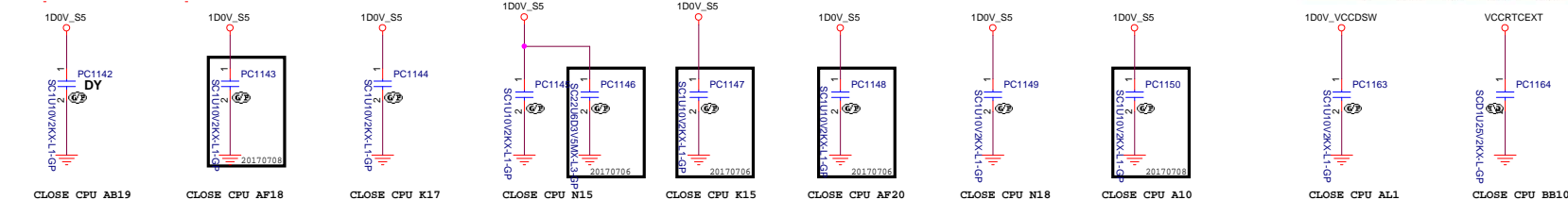
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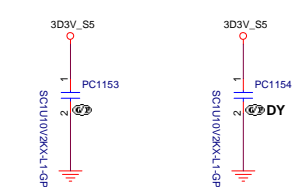
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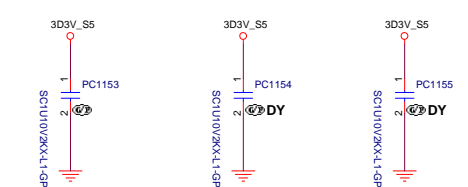
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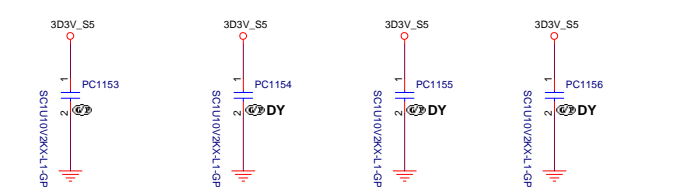
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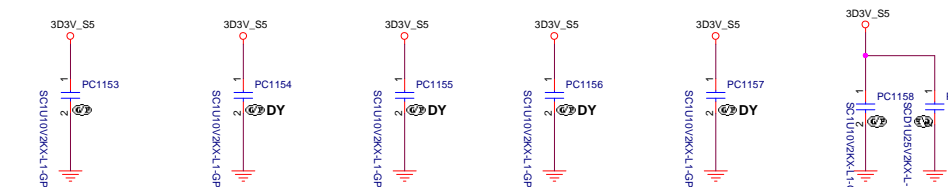
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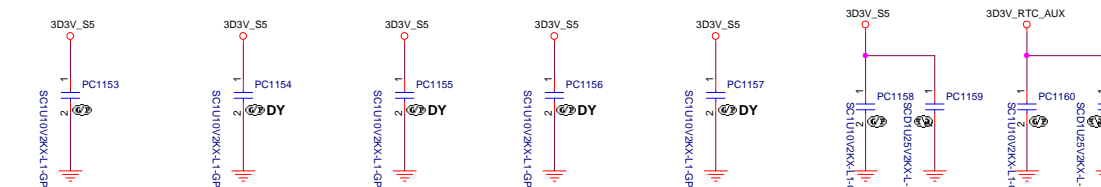
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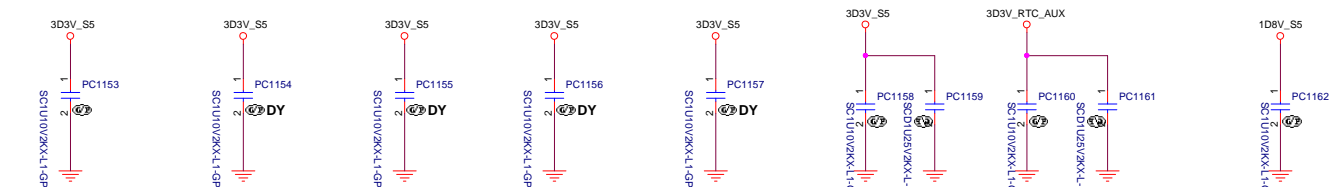
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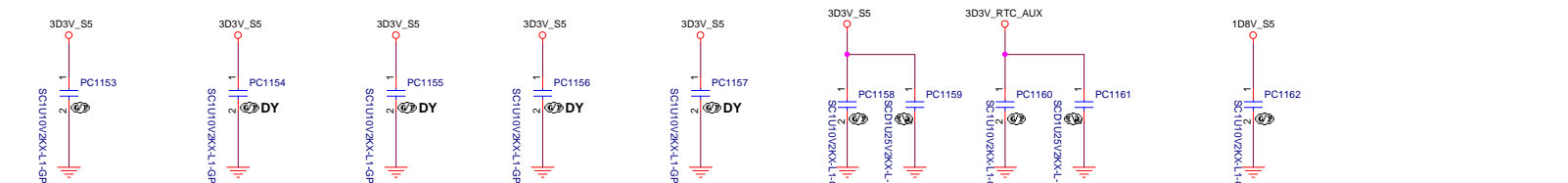
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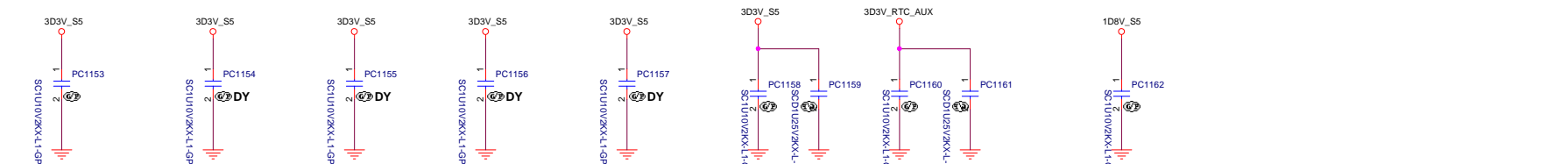
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CLOSE CPU AK17



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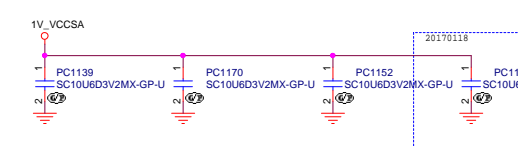
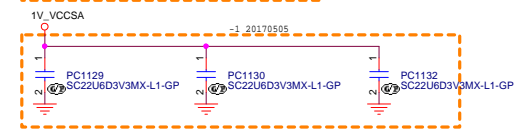
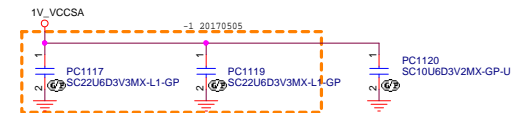
CLOSE CPU AA1

1V\_VCCGT

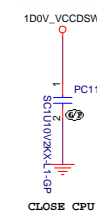
0603 22uF \*14 , 0402 10uF\*26

1V\_VCCSA

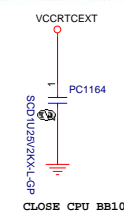
0402 10uF\*12



U22.15W	IA	750KHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mV/30us	1X0.15uH	2X330uF/9mW	30X22uF
	GT	750KHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mV/10us	1X0.15uH	2X330uF/9mW	36X22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mV/30us	1X0.42uH	None	5X22uF



CLOSE CPU AL1



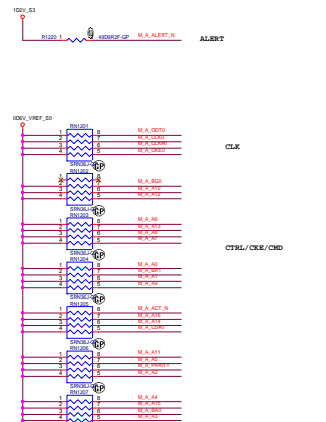
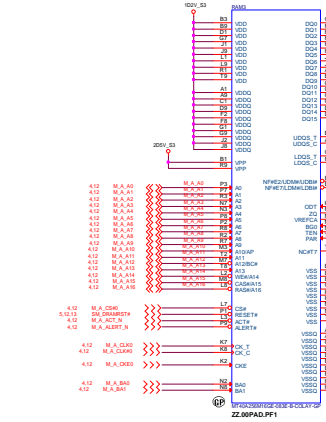
CLOSE CPU BB10

Count

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_(Power CAP2)	
Size Custom	Document Number Woody/Buzz_KBL
Date: Tuesday, July 25, 2017	Sheet 11 of 106

DQ80	DQ0-DQ7
DQ81	DQ8-DQ15
DQ82	DQ16-DQ23
DQ83	DQ24-DQ31
DQ84	DQ32-DQ39
DQ85	DQ40-DQ47
DQ86	DQ48-DQ55
DQ87	DQ56-DQ63

4	M.A.D010	>>>
4	M.A.B00	>>>
4	M.A.D010	>>>



please notice that signal B01 (pin:M9) and U02 (pin:E9) are required

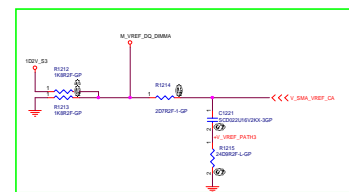
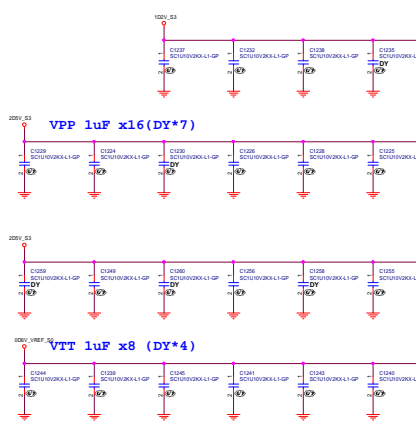
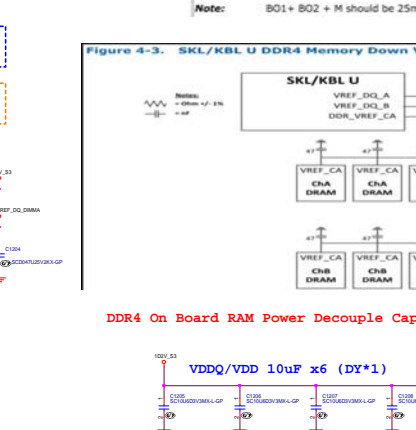
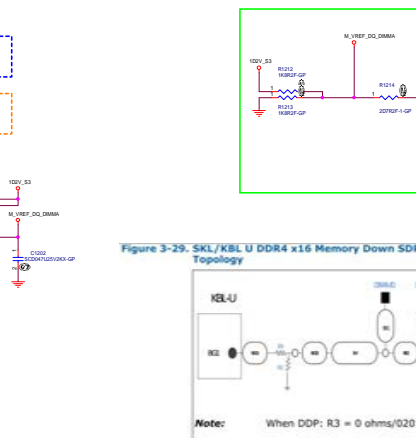
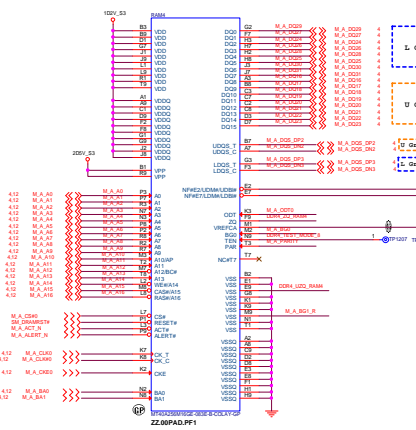
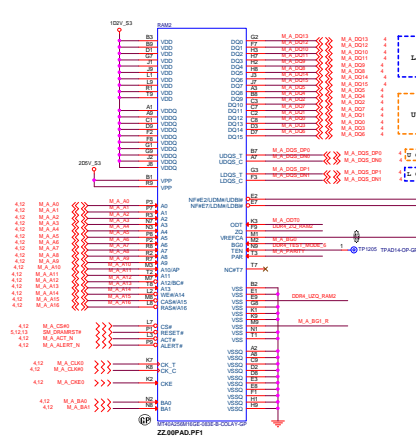
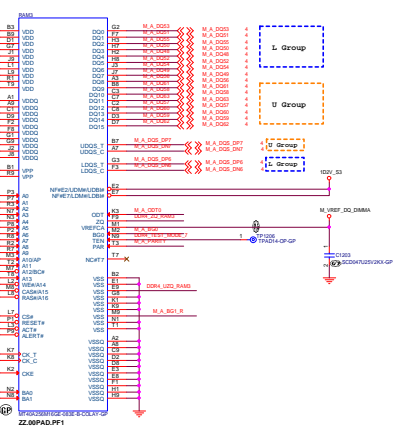
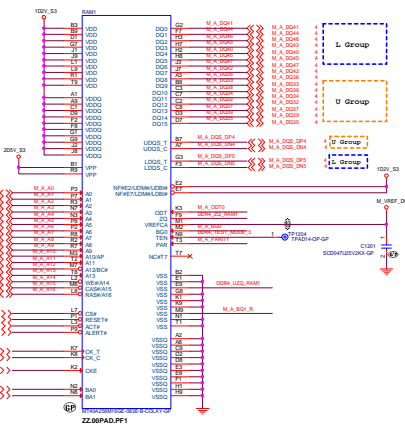


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BGL Signal Topology

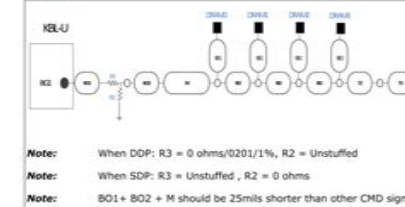
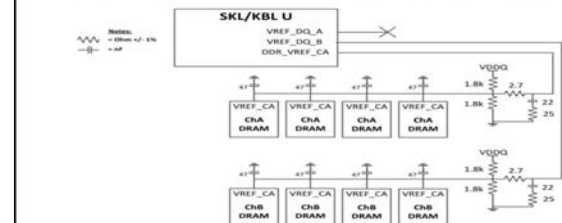
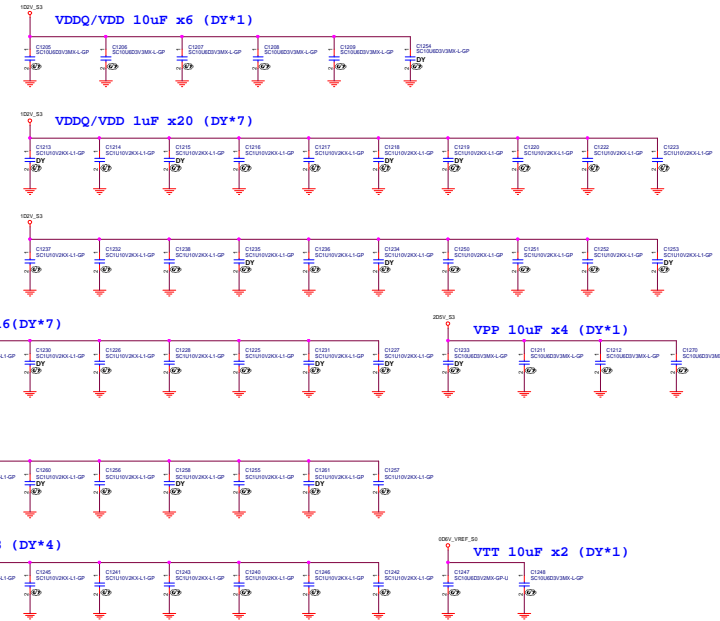


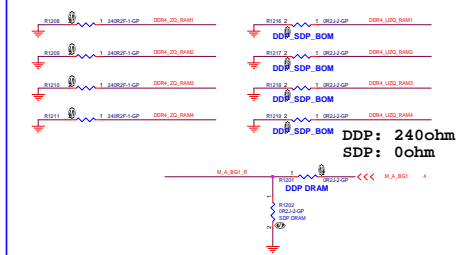
Figure 4-3. SKL/KBL U DDR4 Memory Down VREF-dq and VREF-ca Overview



DDR4 On Board RAM Power Decouple Cap

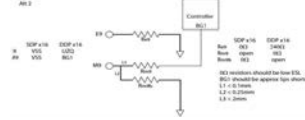


## SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

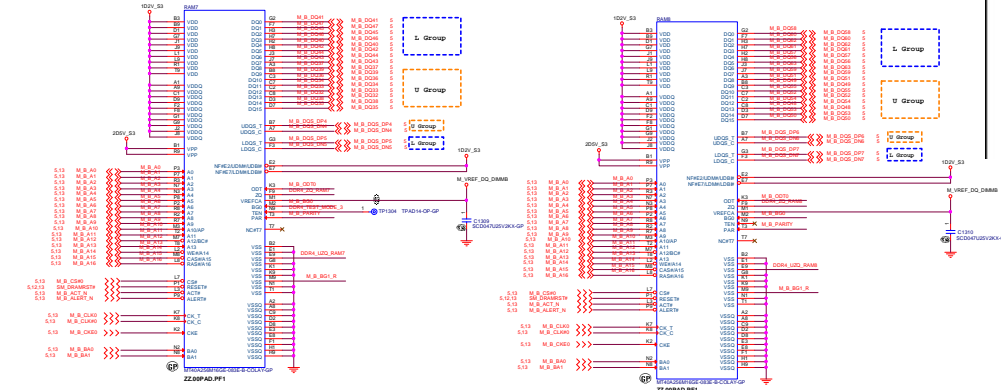
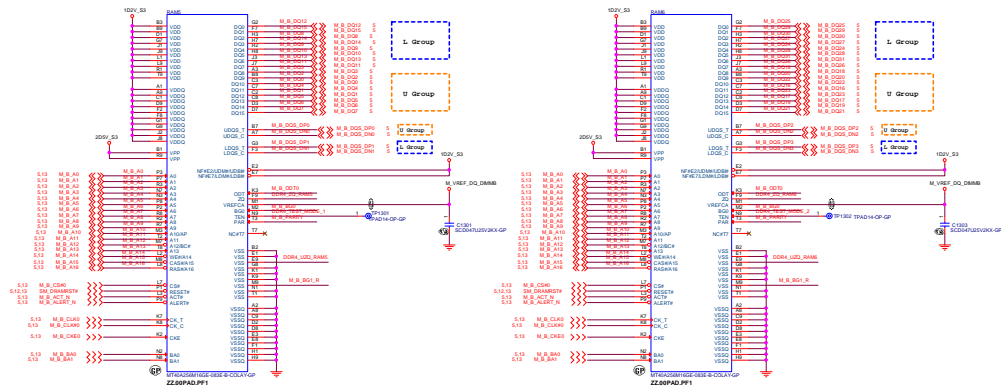
- Alternate two layout, risk of VSS offset increases a little



DQ80	DQ8-DQ7
DQ81	DQ8-DQ15
DQ82	DQ16-DQ23
DQ83	DQ24-DQ31
DQ84	DQ32-DQ39
DQ85	DQ40-DQ47
DQ86	DQ48-DQ55
DQ87	DQ56-DQ63



please notice that signal B01 (pin189) and U02 (pin189) are required



#### 4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1 $\mu$ F (0402)	(All stuffed)
		Distributed around the DRAM devices	10x 10 $\mu$ F (0603)	(All stuffed)
	VPP	2 as near each x16 DRAM device as possible	16x 1 $\mu$ F (0402)	
		Distributed around the DRAM devices	5x 10 $\mu$ F (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1 $\mu$ F (0402)	
		Distributed around the DRAM devices	4x 10 $\mu$ F (0603)	

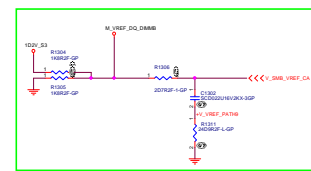
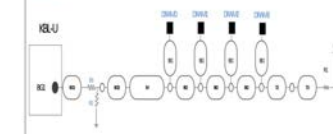
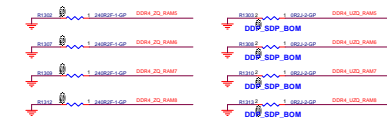


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology



Notes:  
When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed  
When SDP: R3 = Unstuffed, R2 = 0 ohms  
B01 + B02 + M should be 25ms shorter than other CMD signals.

## SDP & DDP SETTING



DDP: 240ohm  
SDP: 0ohm

### DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

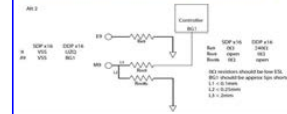
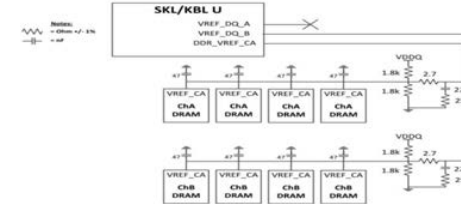
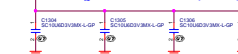


Figure 4-3. SKL/KBL U DDR4 Memory Down VREF-DQ and VREF-CA Overview



### DDR4 On Board RAM Power Decouple Cap

VDDQ/VDD 10uF x6 (DY\*1)



VDDQ/VDD 1uF x20 (DY\*8)



VPP 1uF x16 (DY\*12)



VPP 10uF x4 (DY\*1)



VTT 1uF x6 (DY\*3)



VTT 10uF x2 (DY\*1)





Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved	
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23	
Schematic								
	High	Enable				Enable	eSPI	
	Low	Disable				Disable	LPC	
		internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

DDPB_CTLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/SOP. <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h/Bit 5). 3. This signal is in the primary well.
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GSPI1_MOSI / GPP_B22	Boot BIOS strap bit BBS	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h/Bit 5). 0 = LPC 1 = SPI <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS destination select to LPC by functional strap is in the primary well. This signal will not affect SPI accesses initiated by Intel ME or Integrated GME LAN. 4. This signal is in the primary well.
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Signal	Usage	When Summed	Comment
DDPD_CTLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two GbB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap block size soft strap (hardwired through PTC). <b>Notes:</b> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (BusD, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
----------------	-------------------	--------------------------	---

SMALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
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SMIALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
--------------------	-------------	------------------------	---

Name	Internal Pull-up/ Pull Down (Note 1)	De-Glitch (Note 2)	Multiplexed With	Default	NMI or SPI Capable	Note
		Input	Output			
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None
GPP_B23	20K PD (see note)	Yes	No	SMIALERT# / PCHMOT#	GPO	NMI SPI

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLC	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Internal Pull-down	Internal Pull-down	OFF

## I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low	Driven Low	Driven Low	OFF
SPI0_MOSI	Primary	Internal Pull-up/ Pull-down	Driven Low	Driven Low	OFF
SPI0_MISO	Primary	Internal Pull-up (See Note 1 & 2)	Internal Pull-up	Internal Pull-up	OFF
SPI0_CS0#	Primary	Driven High	Driven High	Driven High	OFF
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	OFF
SPI0_CS2#	Primary	Driven High	Driven High	Driven High	OFF
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	OFF
SPI1_CLK	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MISO	Primary	Undriven	Undriven	Undriven	OFF
SPI1_CS#	Primary	Undriven	Undriven	Undriven	OFF
SPI1_IO[2:3]	Primary	Undriven	Undriven	Undriven	OFF

**Notes:**  
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.  
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

Cont

Wistron Corporation  
2/F, 88, Sec. 1, Hsin-Feng Rd., Hsinchu, Taiwan 301, Taiwan, R.O.C.

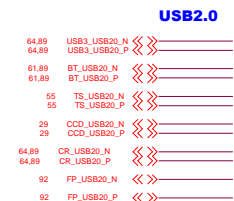
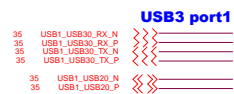
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Woody/Buzz\_KBL

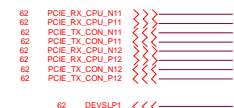
Rev: 1.00, 2019.07.20

Page 11 of 18

5  
Main Func = PCH



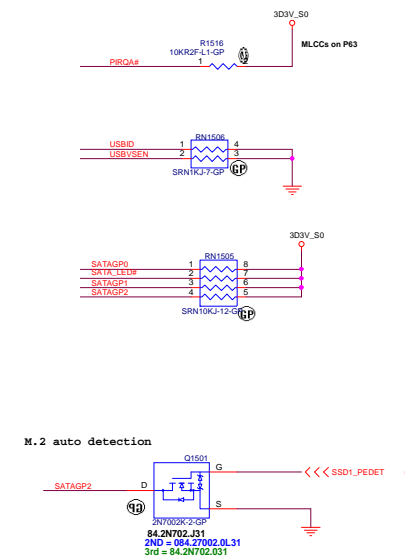
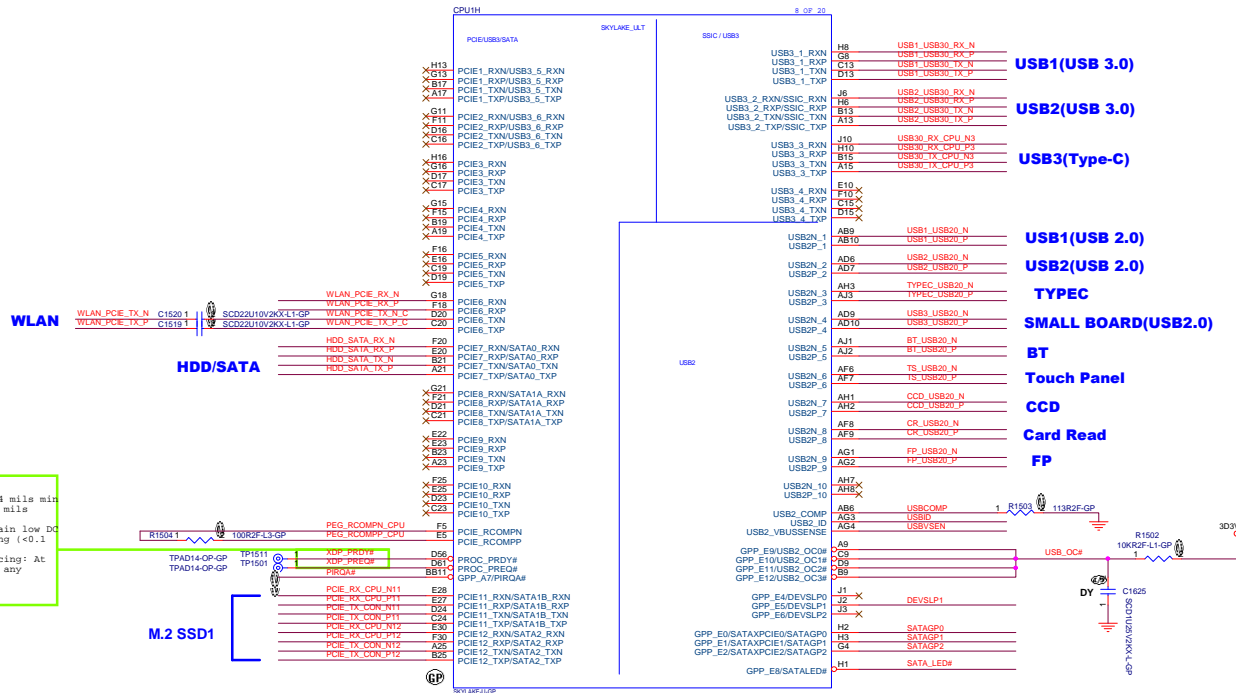
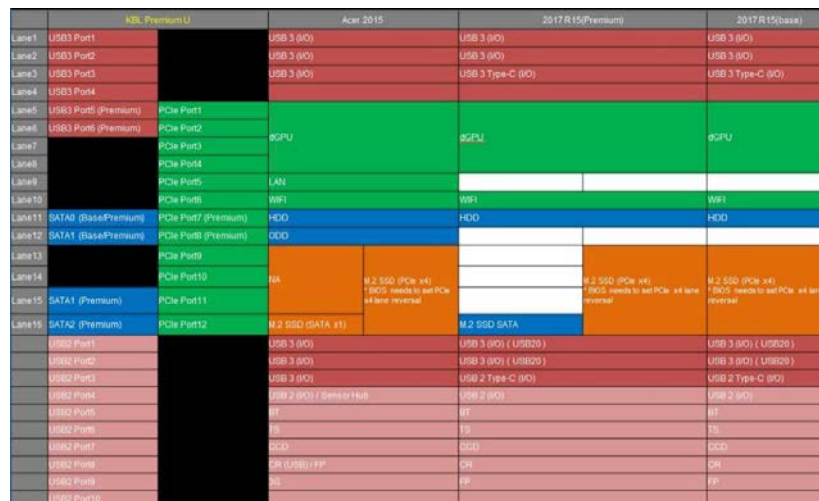
## M.2



## HDD



## WLAN



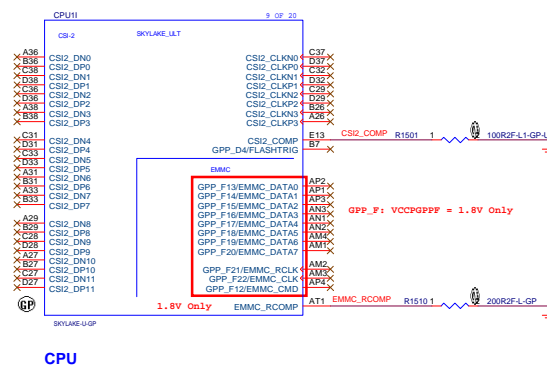
Pin define from PCH and socket side

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

**\*\* Native: Internal Pull-Up (15k-40k) when function.**

Table 27. Socket 2 Module Configuration

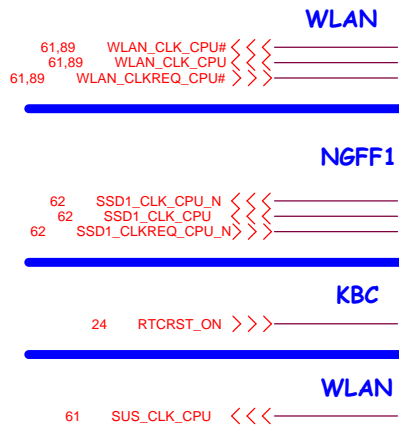
State #	Module Configuration Decodes				Module Type and Main Host Interface <sup>1</sup>	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A



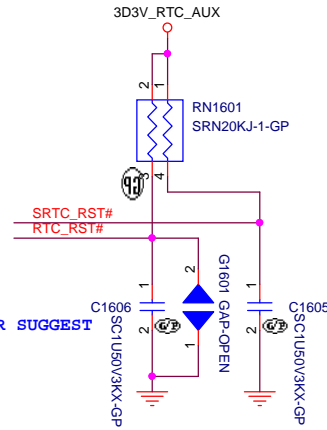
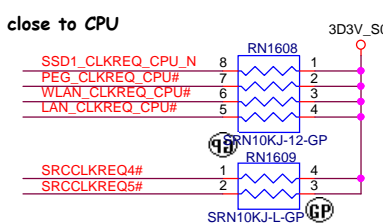
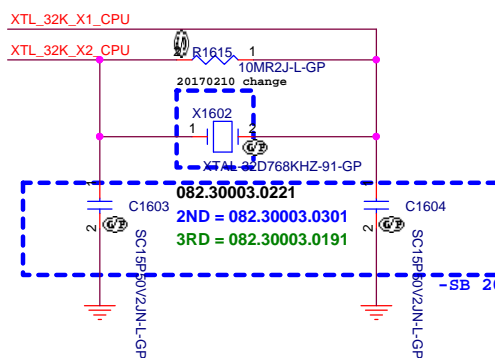
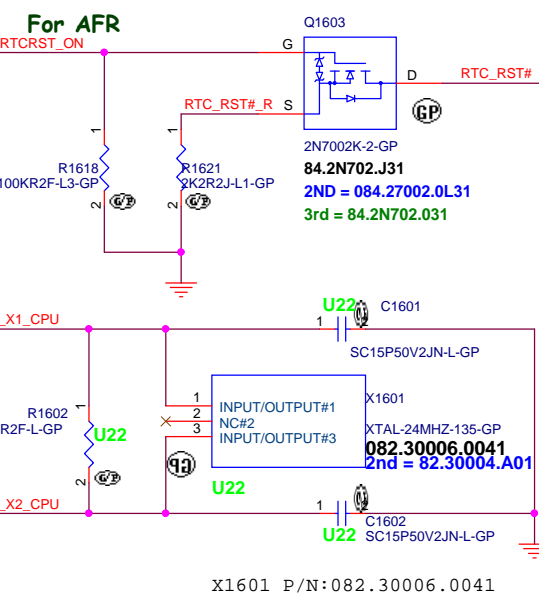
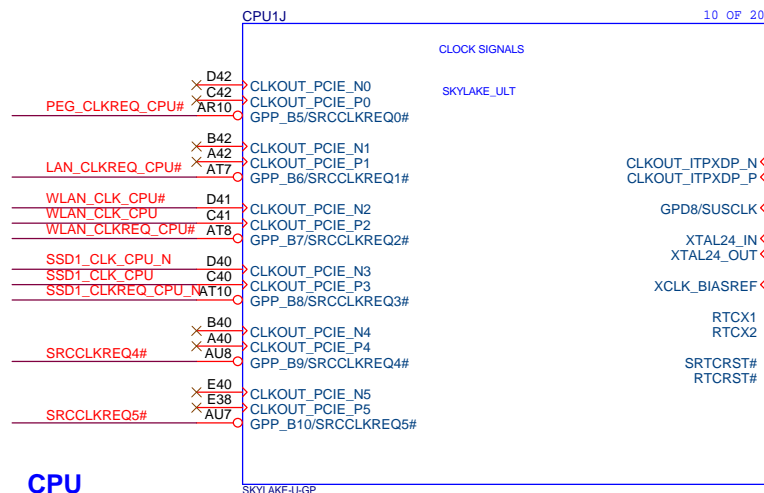
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Size Custom	Document Number	<b>Woody/Buzz_KBL</b>	Rev <b>-2</b>
Date:	uesday, July 25, 2017	Sheet	15 of 106



Main Func = PCH



WLAN  
NGFF1



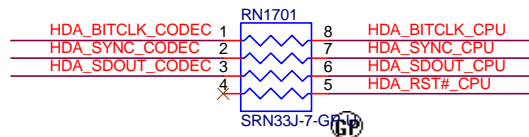
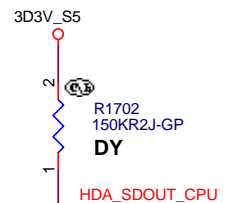
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		MCP_CLOCK	
Size	Document Number	Woody/Buzz_KBL	
Custom		-2	
Date:	tuesday, July 25, 2017	Sheet	16 of 106

# Main Func = PCH

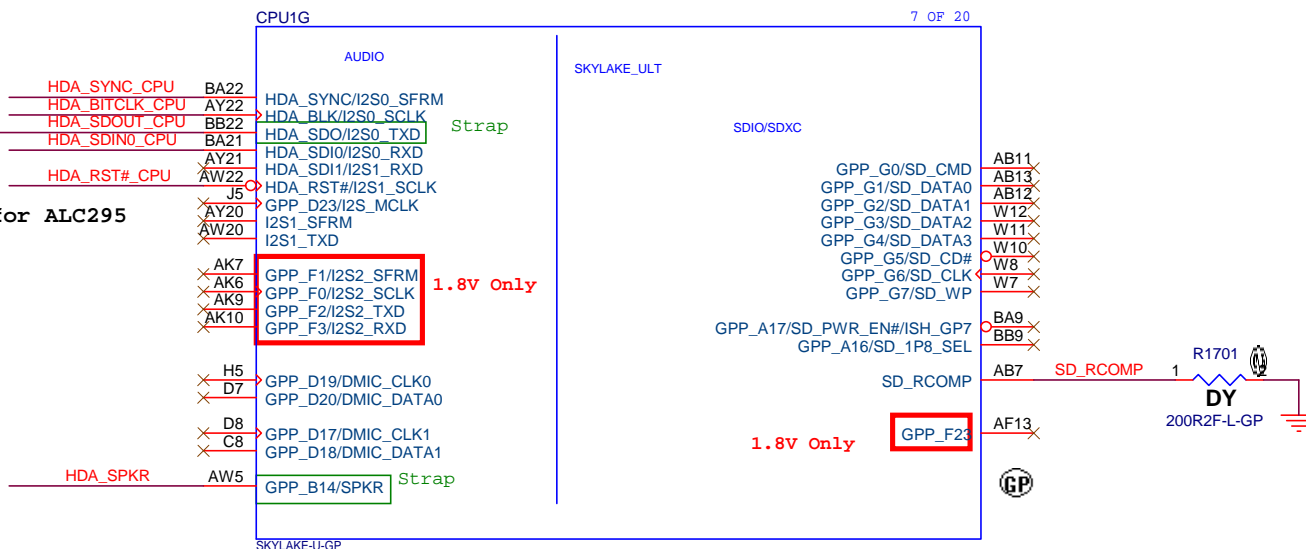
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27 HDA\_SYNC\_CODEEC <<<< \_\_\_\_\_  
27 HDA\_BITCLK\_CODEEC <<<< \_\_\_\_\_  
27 HDA\_SDOUT\_CODEEC <<<< \_\_\_\_\_  
27 HDA\_SDIN0\_CPU <<<< \_\_\_\_\_  
14,27 HDA\_SPKR <<<< \_\_\_\_\_

24 ME\_UNLOCK <<<< \_\_\_\_\_



RESET# in not required for ALC295



## 18.3 Terminating Unused SDXC Signals

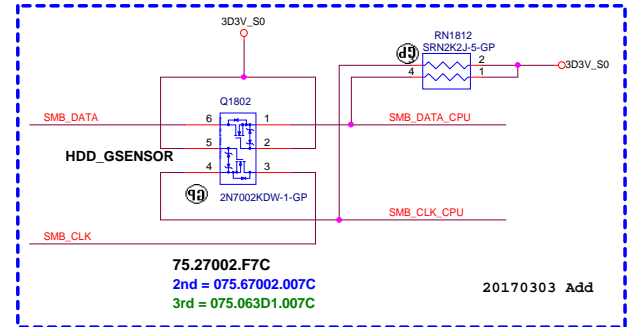
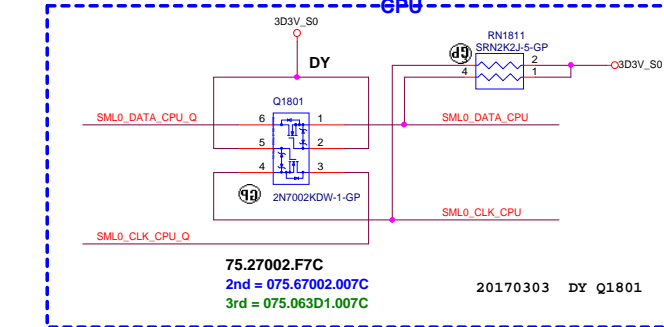
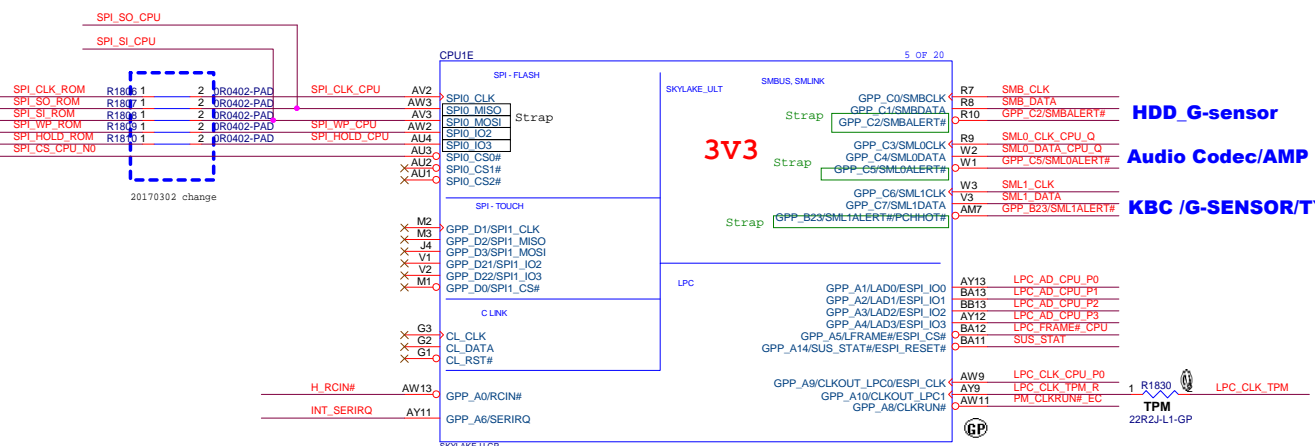
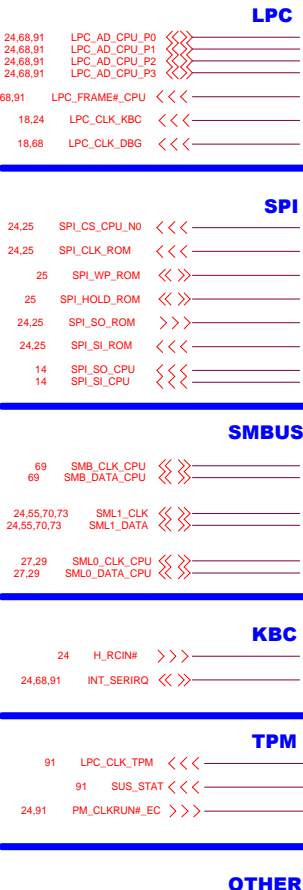
SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD\_RCOMP pin does not need to be connected to a RCOMP resistor.

Count

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_(AUDIO/SDIO/SDXC)	
Size Custom	Document Number Woody/Buzz_KBL
Date: Tuesday, July 25, 2017	Rev -2
Sheet 17	of 106

Main Func = PCH



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.
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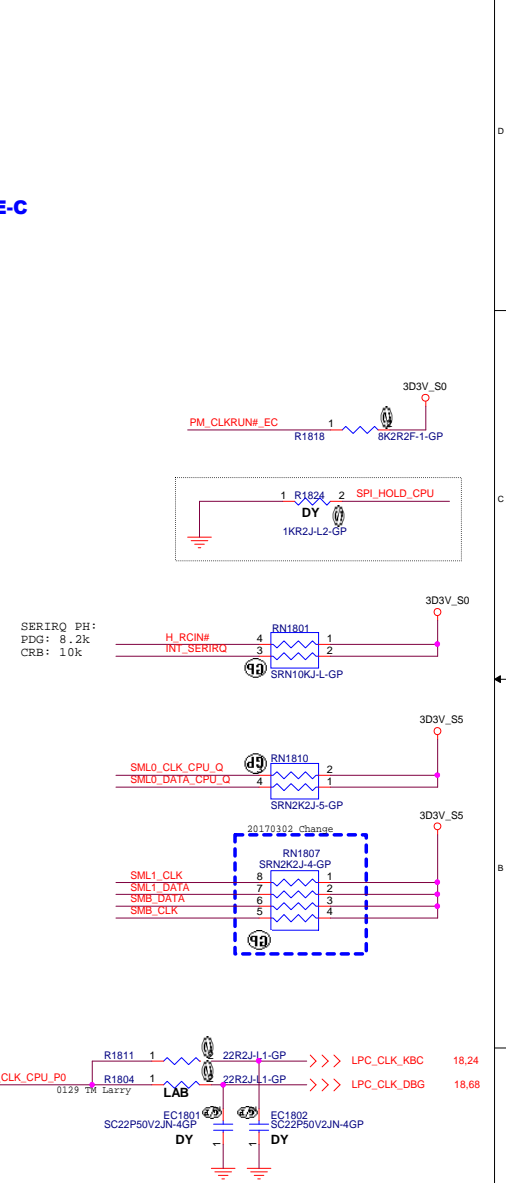
20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT\_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase**, Signal driven low
- **R – Recovery Phase**, Signal driven high
- **T – Turn-around Phase**, Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

**Note:** IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.



Count

緯創資通 Wistron Corporation  
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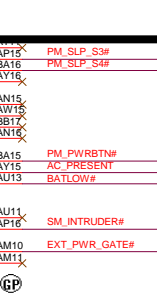
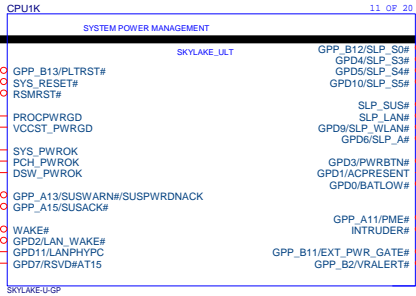
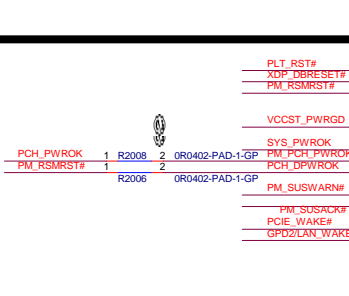
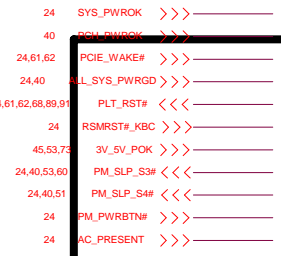
Title **LPC,SPI,SMBUS,CLINK**

Size Custom Document Number **Woody/Buzz\_KBL** Rev **-2**

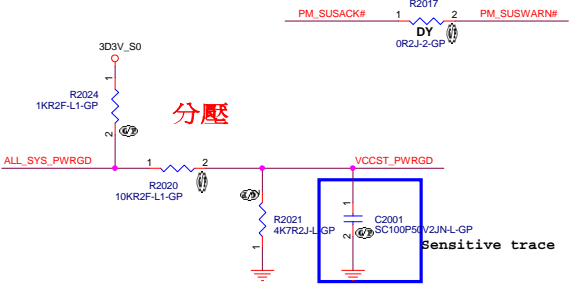
Date: Tuesday, July 25, 2017 Sheet 18 of 106



Main Func = PCH



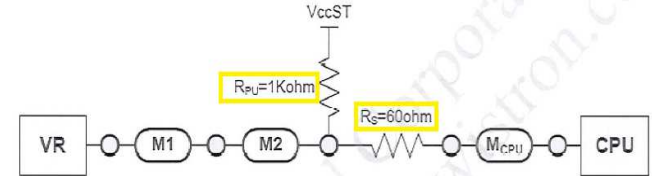
BATLOW##: Pull-up required even if not implemented.



#54306 Rev0.7  
1. VCCST\_PWRGD is only 1.0 V tolerant.  
2. VCCST\_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

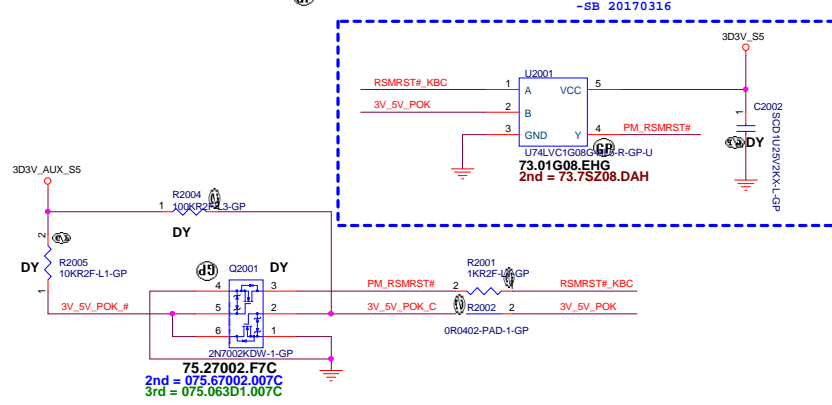
VCCST\_PWRGD / HWM201:

VCCST\_PWRGOOD



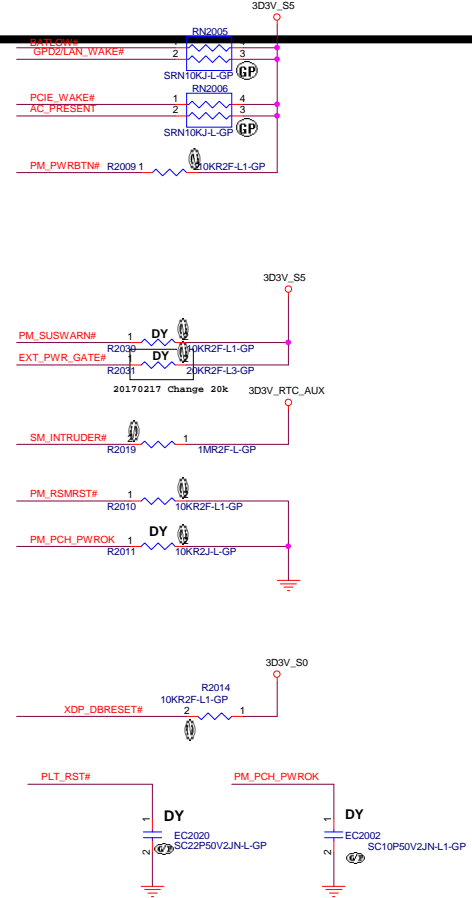
VCCST\_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

CPU



GPP\_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN# / SUSPWRDNACK eSPI mode: None	SUSWARN# / SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

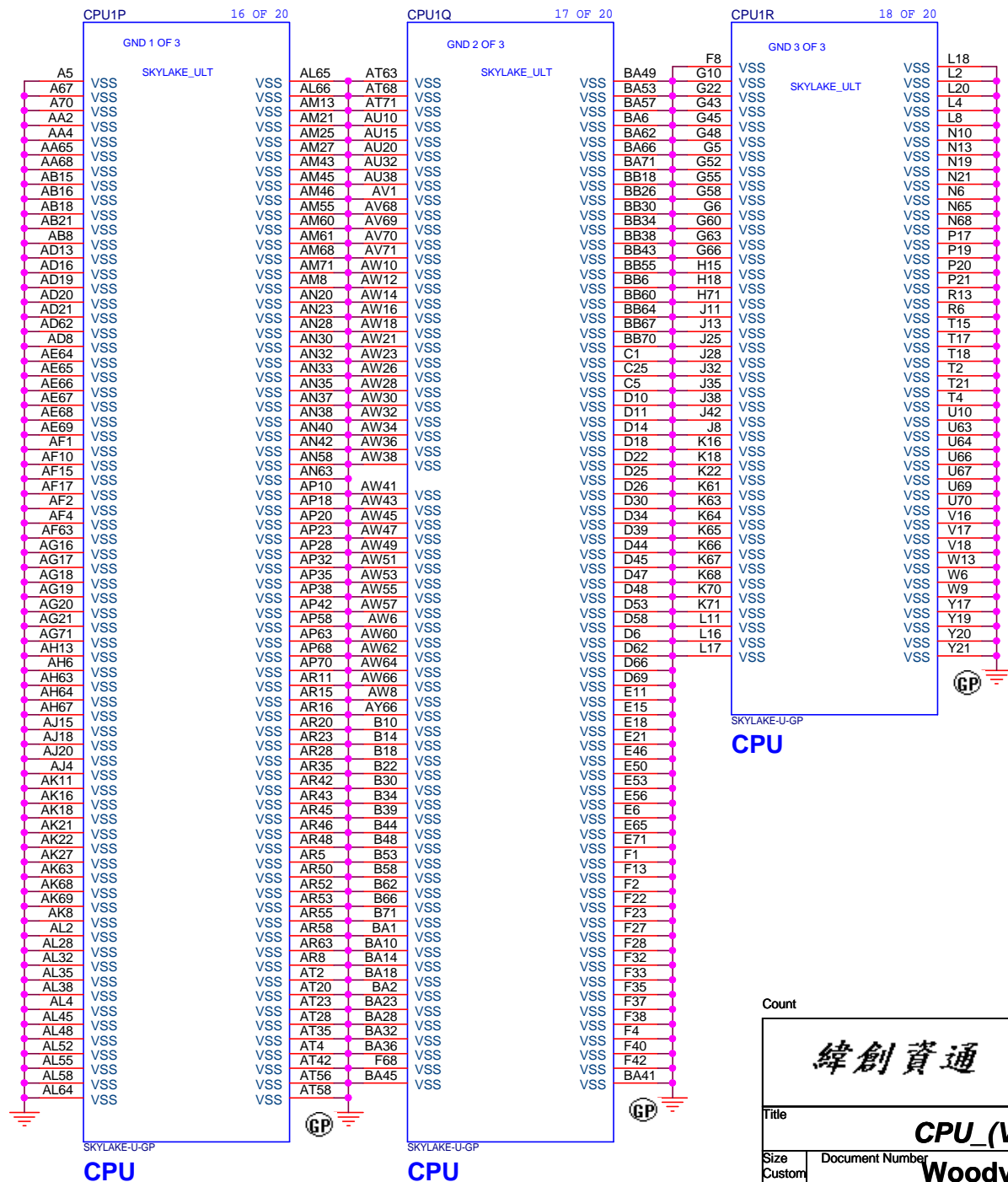


Count

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title CPU\_(POWER MANAGEMENT)  
Size Custom Document Number Woody/Buzz\_KBL Rev -2  
Date: Tuesday, July 25, 2017 Sheet 20 of 106

Main Func = PCH



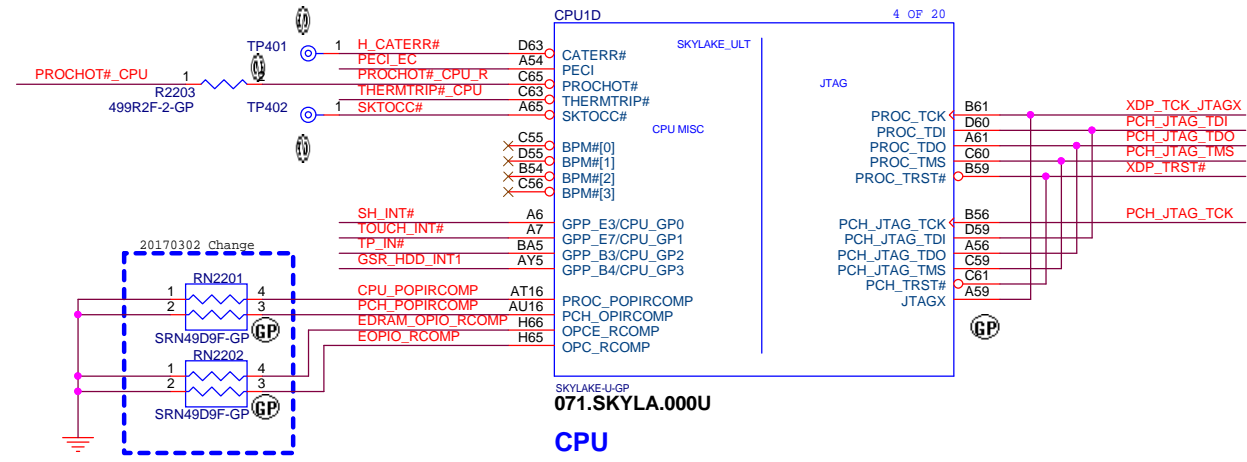
Count

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU_(VSS)		
Size Custom	Document Number Woody/Buzz_KBL	Rev -2
Date: Tuesday, July 25, 2017	Sheet 21	of 106

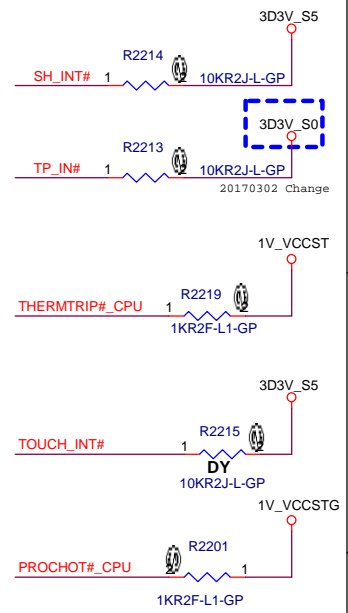
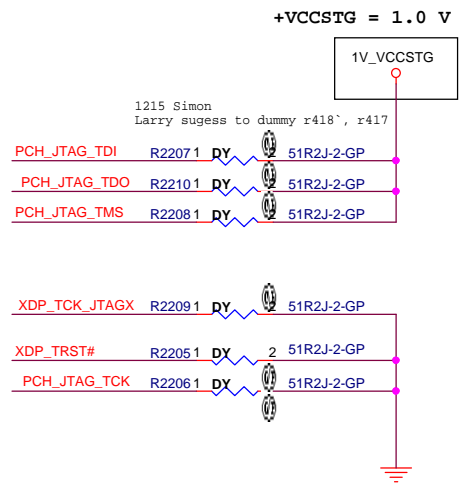


Main Func = CPU

- 24 Peci\_EC <<>>
- 24,44,46 Prochot#\_CPU <<>>
- 24 SH\_INT# >>>
- 55 Touch\_Int# >>>
- 65 TP\_IN# >>>
- 69 GSR\_HDD\_INT1 >>>



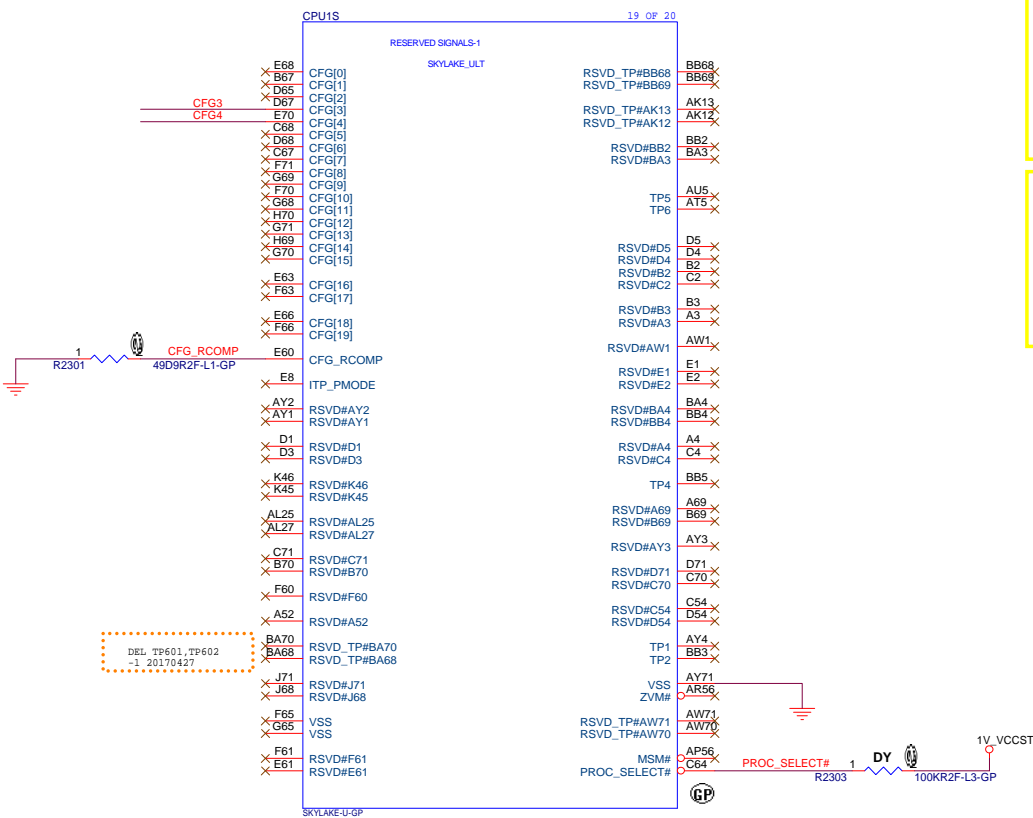
PROCHOT#	<b>Processor Hot:</b> PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GT L OD 0	SE	All processor lines
THERMTRIP#	<b>Thermal Trip:</b> The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	0	OD	SE	All processor lines



Count	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_(JTAG/CPU SIDE BAND)	
Size Custom	Document Number Woody/Buzz KBL
Date: Tuesday, July 25, 2017	Rev -2
Sheet 22 of 106	



Main Func = CPU



CPU

CPU

**PCH strap pin:**

CFG3

R2305 1KR2J-1-GP

CFG3

[BDW Only] PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

**PCH strap pin:**

CFG4

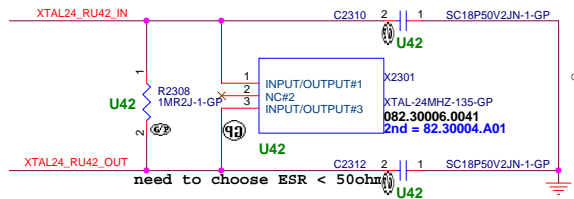
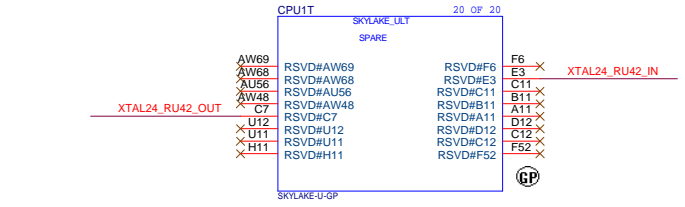
R2304 1KR2J-1-GP

CFG4

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"><li>• <b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none"><li>– 1 = (Default) Normal Operation; No stall.</li><li>– 0 = Stall.</li></ul></li><li>• <b>CFG[1]:</b> Reserved configuration lane.</li><li>• <b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none"><li>– 1 = Normal operation</li><li>– 0 = Lane numbers reversed.</li></ul></li><li>• <b>CFG[3]:</b> Reserved configuration lane.</li><li>• <b>CFG[4]:</b> eDP enable:<ul style="list-style-type: none"><li>– 1 = Disabled.</li><li>– 0 = Enabled.</li></ul></li><li>• <b>CFG[6:5]:</b> PCI Express* Bifurcation<ul style="list-style-type: none"><li>– 00 = 1 x8, 2 x4 PCI Express*</li><li>– 01 = reserved</li><li>– 10 = 2 x8 PCI Express*</li><li>– 11 = 1 x16 PCI Express*</li></ul></li><li>• <b>CFG[7]:</b> PEG Training:<ul style="list-style-type: none"><li>– 1 = (default) PEG Train immediately following RESET# de assertion.</li><li>– 0 = PEG Wait for BIOS for training.</li></ul></li><li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li></ul>	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.
-----------	---	-----	-----	----	---

PROC_SELECT#	<b>Processor Select:</b> This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines
--------------	---	--	--	-----	---------------------



P/N: 082.30006.0041

**D**

B

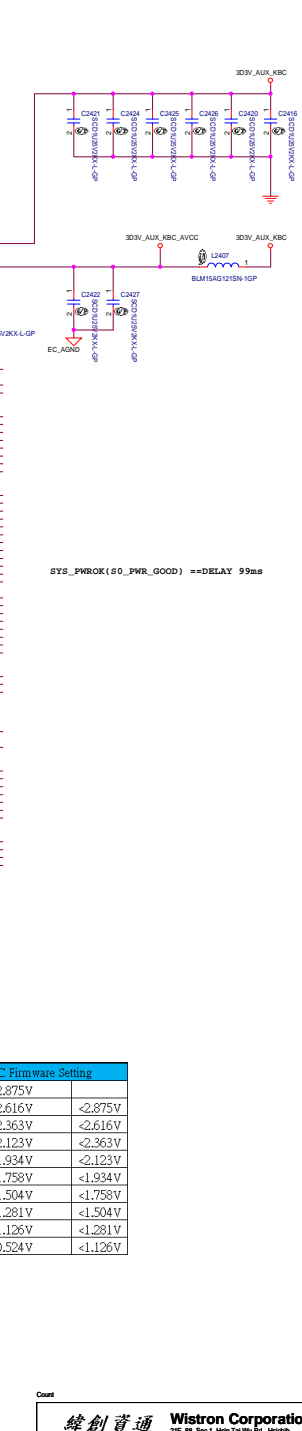
A

4

3

2

1

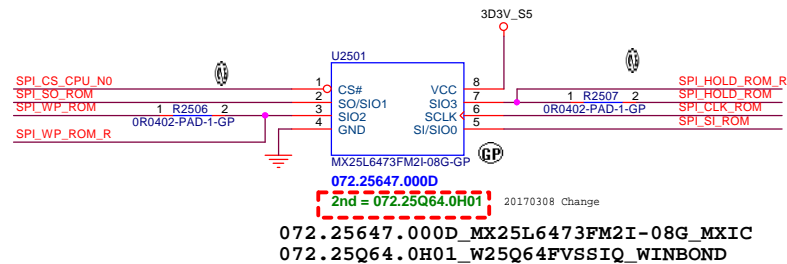
[illegible]

Count		緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
KBC KB9028		Rev	
Size	Document Number	Woody/Buzz KBL	
Custom		-2	
Date:	100509, July 25, 2017	Sheet	24 of 106

## Main Func = SPI Flash

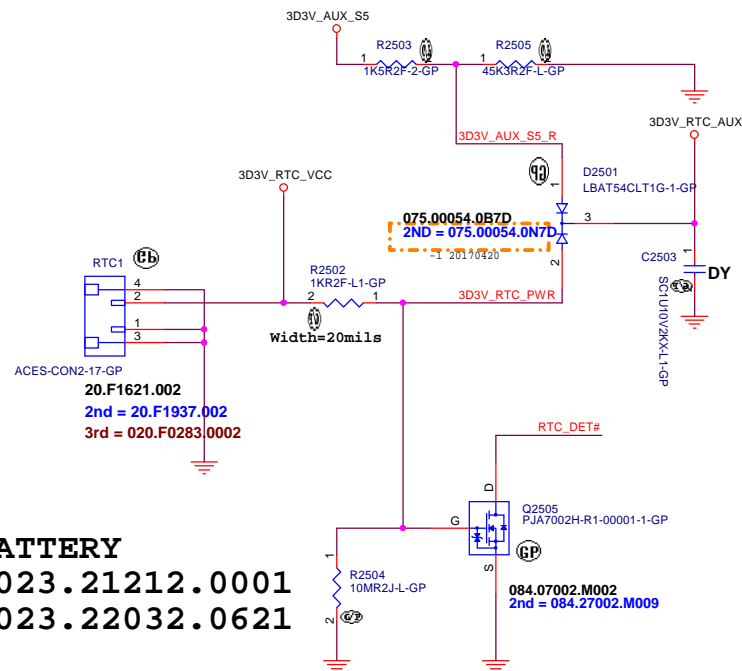
### SPI FLASH ROM (8M byte) for PCH

*SPI ROM Equal length need to less than 500mil*



20170215 Delete U2504 For ENG

## Main Func = RTC



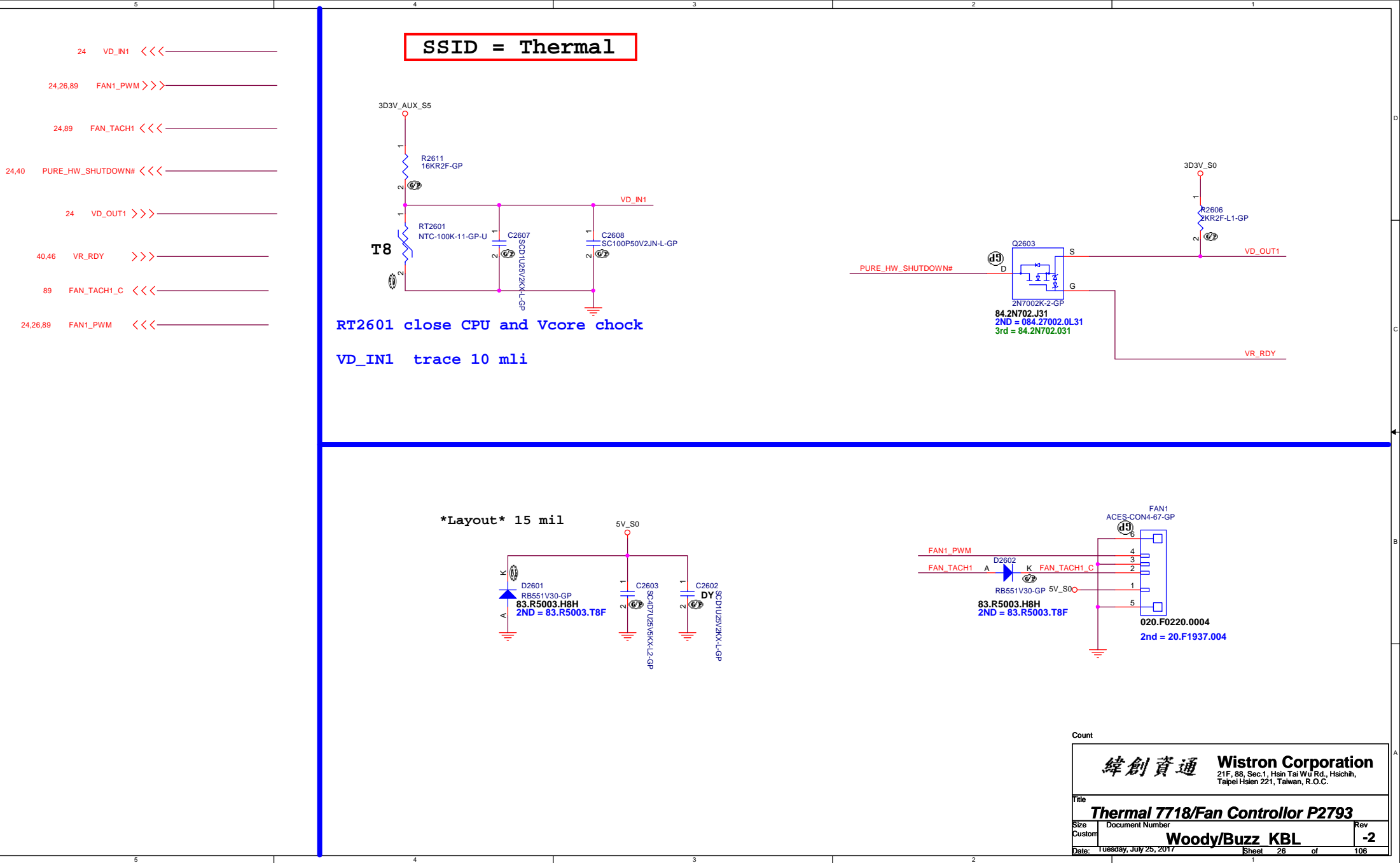
### RTC BATTERY

1st= 023.21212.0001

2nd= 023.22032.0621

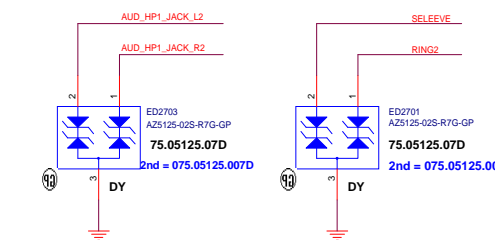
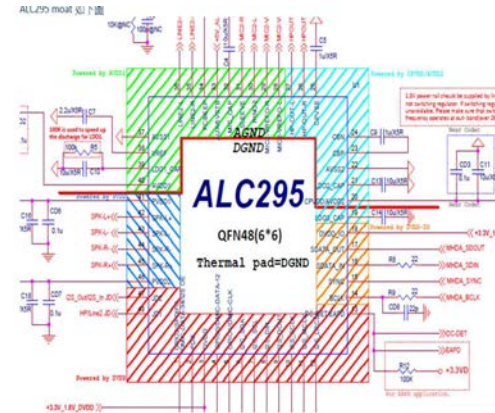
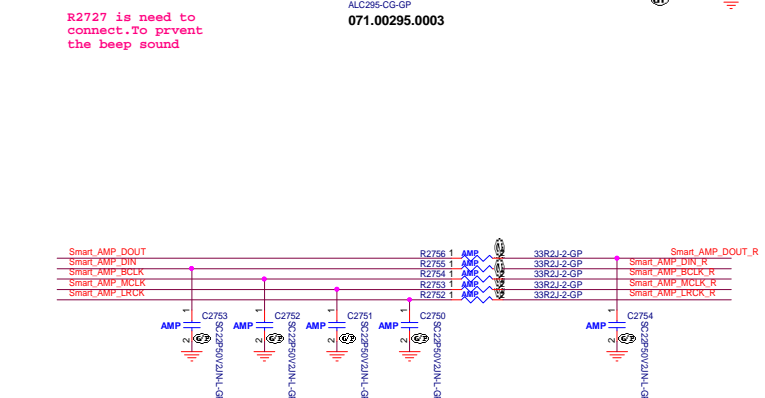
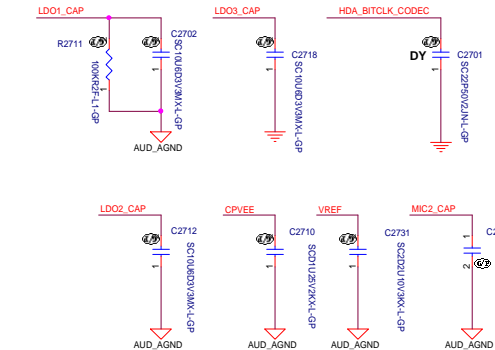
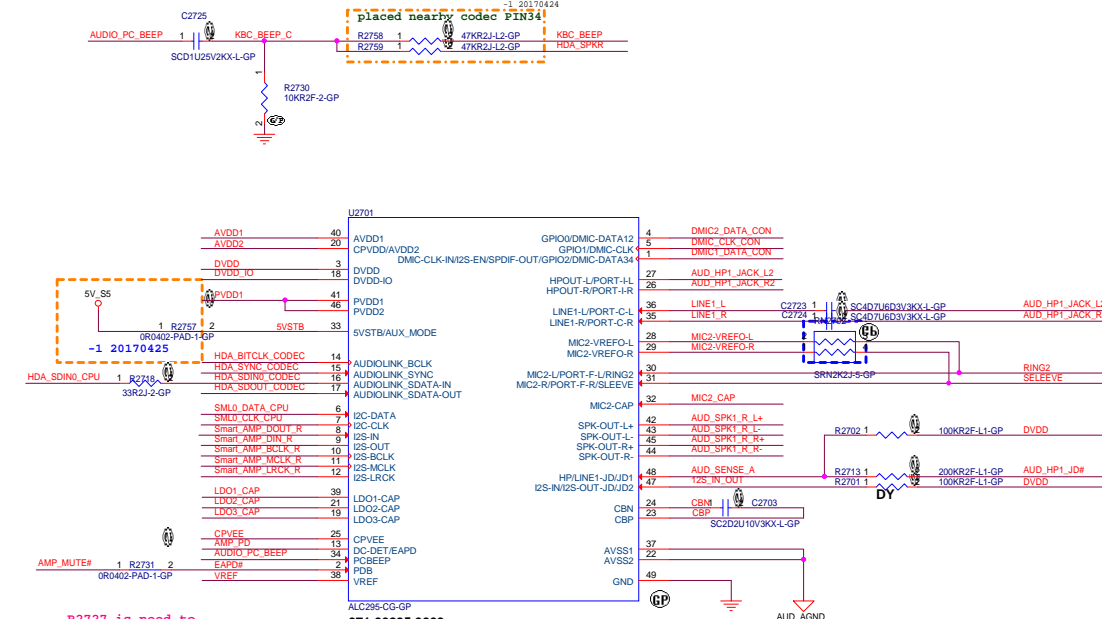
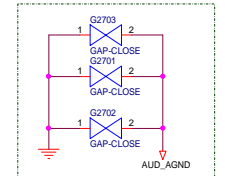
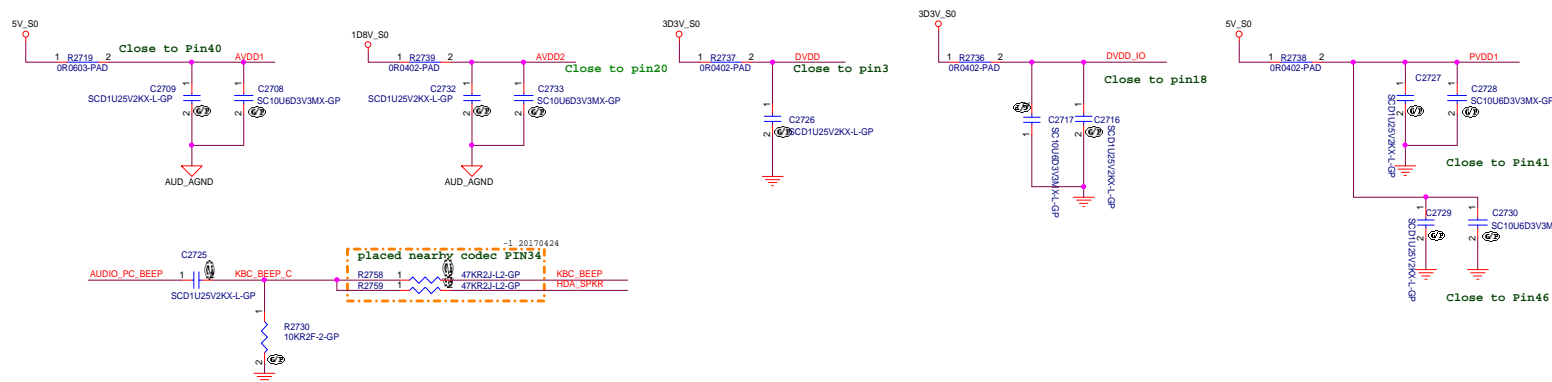
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Flash(KBC+PCH)/RTC</b>			
Size	Document Number		Rev
Custom		<b>Woody/Buzz KBL</b>	<b>-2</b>
Date:	Tuesday, July 25, 2017	Sheet 25 of	106



# SSID = AUDIO

29.89 AUD\_SPK1\_R\_L+ <<<  
 29.89 AUD\_SPK1\_R\_L- <<<  
 29.89 AUD\_SPK1\_R\_R+ <<<  
 29.89 AUD\_SPK1\_R\_R- <<<  
 17 HDA\_BITCLK\_CODEC >>>  
 17 HDA\_SYNC\_CODEC >>>  
 17 HDA\_SDIN0\_CPU <<<  
 17 HDA\_SDOUT\_CODEC >>>  
 18.29 SML0\_DATA\_CPU >>>  
 18.29 SML0\_CLK\_CPU >>>  
 29 AMP\_PD <<<  
 24 KBC\_BEEP >>>  
 14,17 HDA\_SPKR >>>  
 24 AMP\_MUTE# >>>  
 29 DMIC2\_DATA\_CON >>>  
 29 DMIC\_CLK\_CON >>>  
 29 DMIC1\_DATA\_CON >>>  
 64.89 AUD\_HP1\_JACK\_L2 <<<  
 64.89 AUD\_HP1\_JACK\_R2 <<<  
 64.89 AUD\_HP1\_ID# >>>  
 64.89 RING2 >>>  
 64.89 SELEEVE >>>  
 29 Smart\_AMP\_DOUT >>>  
 29 Smart\_AMP\_DIN >>>  
 29 Smart\_AMP\_BCLK >>>  
 29 Smart\_AMP\_MCLK >>>  
 29 Smart\_AMP\_LRCLK >>>



Blanking

Count

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

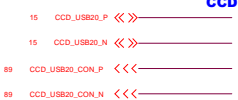
**Woody/Buzz KBL**

Rev  
**-2**

Date: Tuesday, July 25, 2017

Sheet 28 of 106

**SSID = AUDIO**

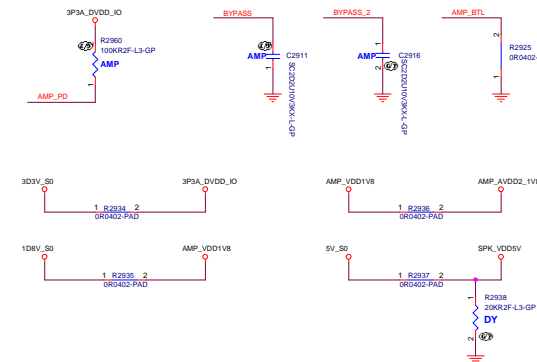
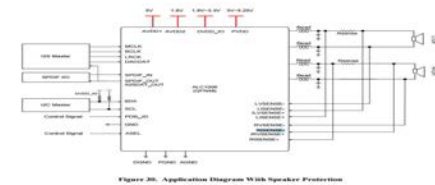
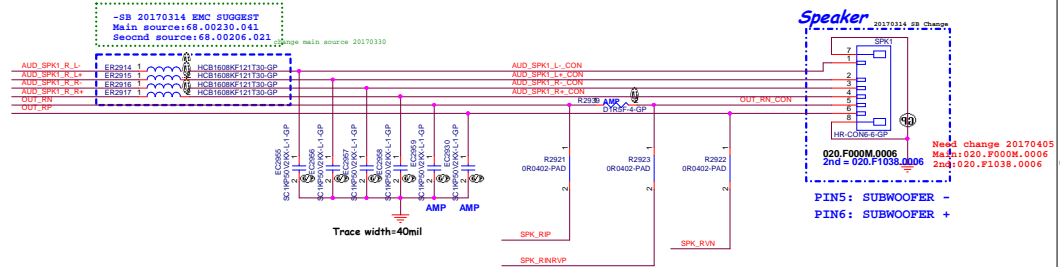
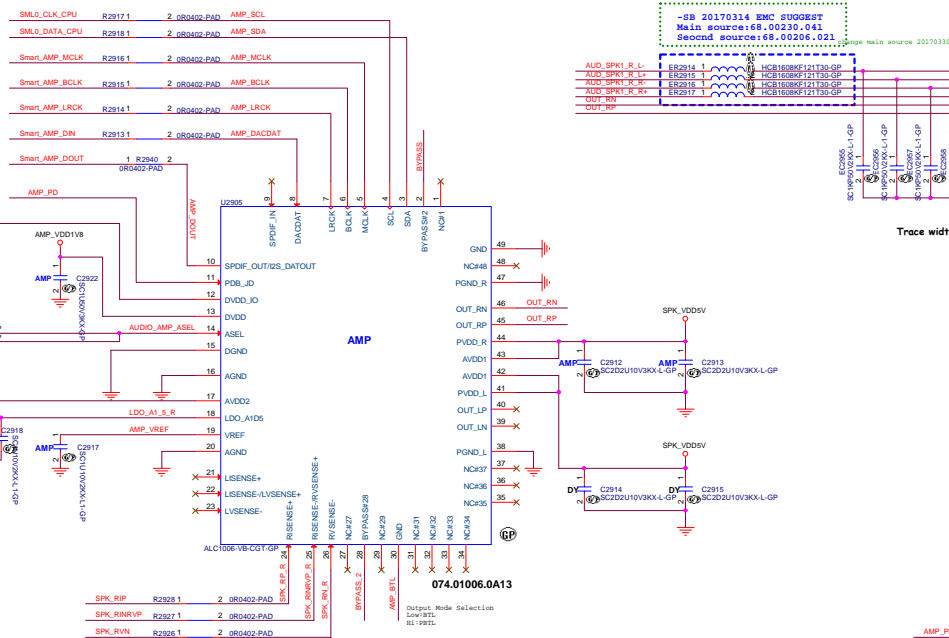
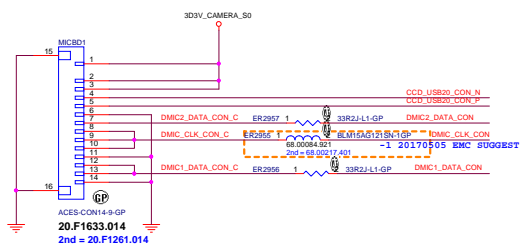
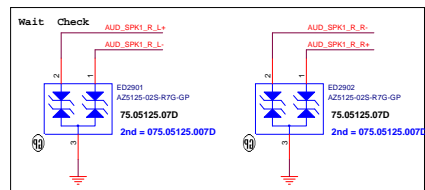


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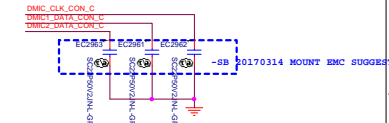
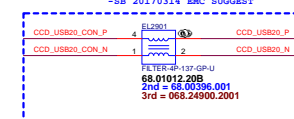
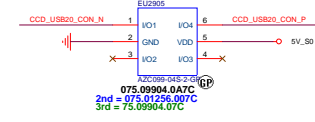
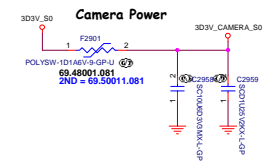
27  DMIC_CLK_CON >>>—————
27  DMIC1_DATA_CON >>>—————
27  DMIC2_DATA_CON >>>—————

89  DMIC_CLK_CON_C <<<—————
89  DMIC1_DATA_CON_C <<<—————
89  DMIC2_DATA_CON_C <<<—————

```



A. Pin define		Note	
CCD Module			
MB Connector		CCD connector pin	MIC-R PCB
Pin 1	303V CAMERA S0	1	
Pin 2	303V CAMERA S0		1
Pin 3	303V CAMERA S0		
Pin 4	CCD_USB20_CON_N	2	
Pin 5	CCD_USB20_CON_P	3	
Pin 6	GND	4	
Pin 7	DMIC2_DATA_CON	6	
Pin 8	DMIC_CLK_CON	5	
Pin 9	DMIC_CLK_CON		3
Pin 10	DMIC_CLK_CON		
Pin 11	GND		4
Pin 12	DMIC1_DATA_CON		2
Pin 13	DMIC1_DATA_CON		
Pin 14	GND		2
			4
MB Connector		CCD Connector	





# Blanking

Count

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Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

**Woody/Buzz KBL**

Rev  
**-2**

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# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>		Sheet <div>31</div> of <div>106</div>

Blanking

Count		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	Woody/Buzz KBL	-2
Date:	Tuesday, July 25, 2017	Sheet 32 of 106


# Blanking

Count

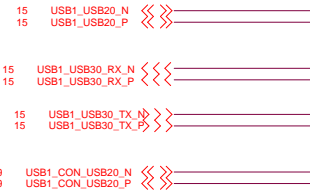
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>	Sheet <div>33</div> of <div>106</div>	

# Blanking

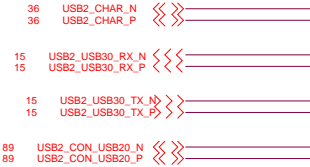
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>Woody/Buzz KBL</b>		Rev <b>-2</b>
Date: Tuesday, July 25, 2017		Sheet 34 of	106

## USB1



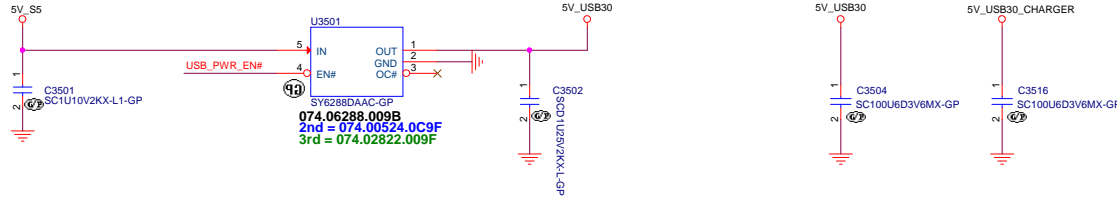
## USB2



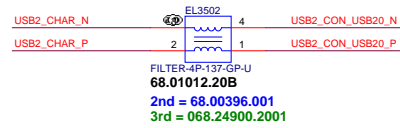
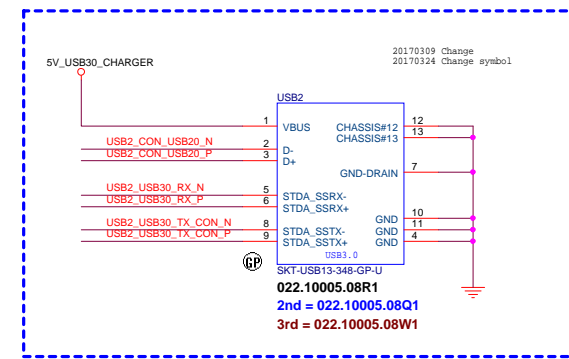
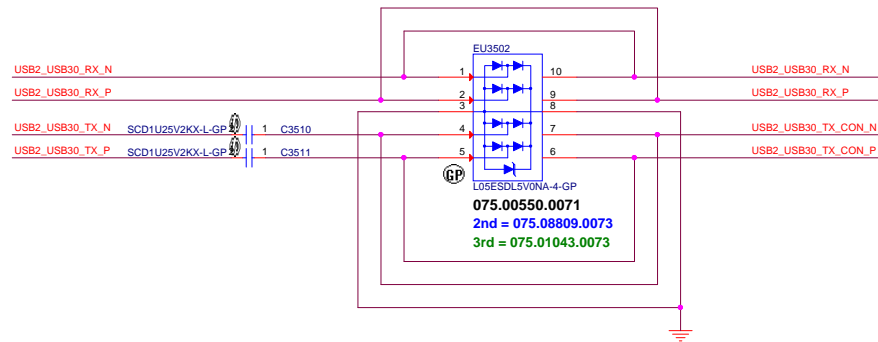
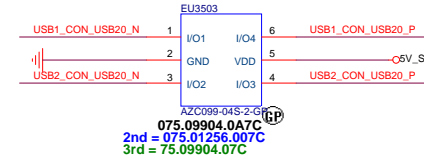
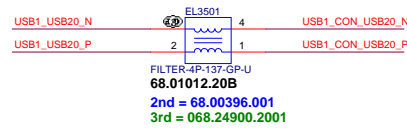
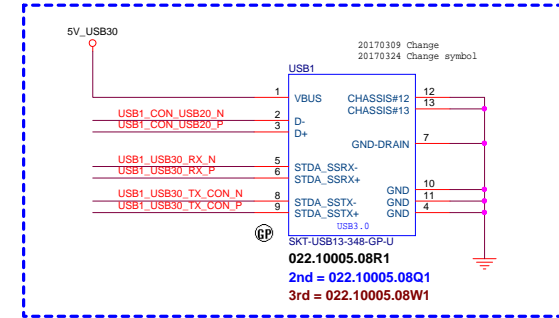
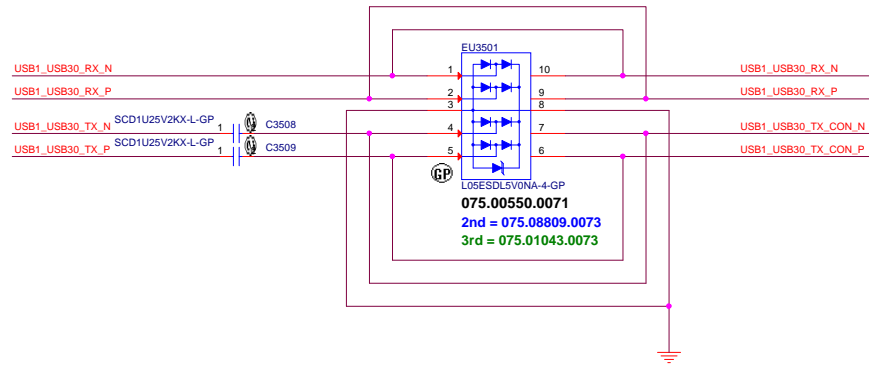
## USB Power enable



## Low Active 2A



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



Count

<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Heilinh, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>File USB 3.0</p>		
Size	Document Number	Rev
Custom	Woody/Buzz KBL	-2
Date: Tuesday, July 25, 2017	Sheet 35	of 106

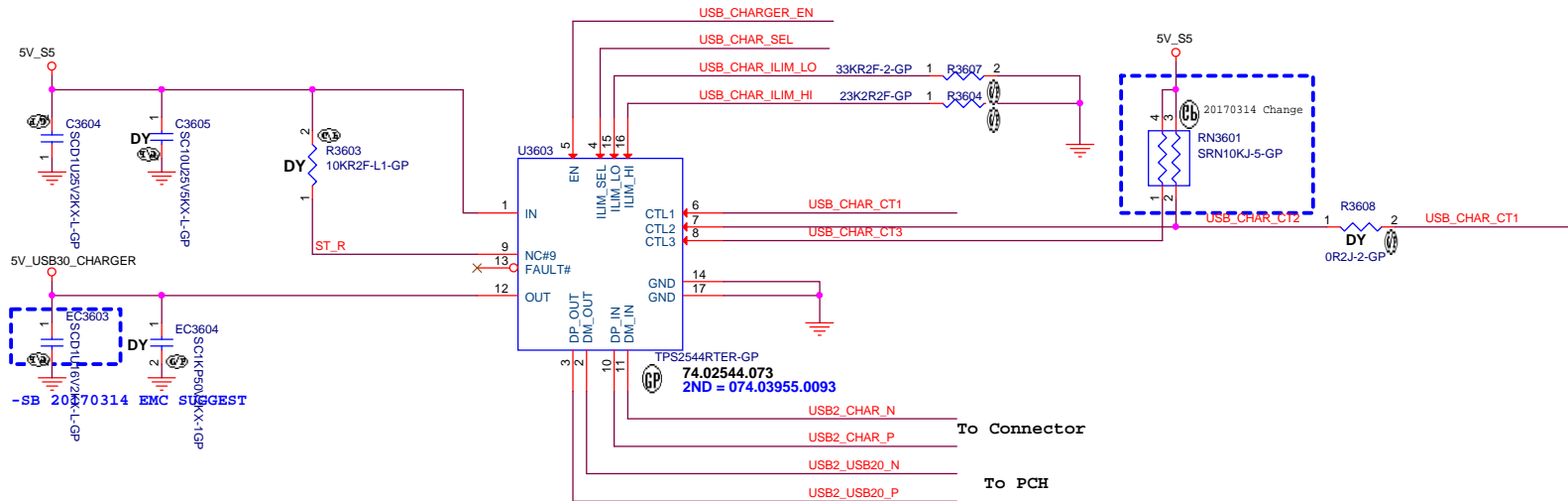
24 USB\_CHARGER\_EN >>>  
 24 USB\_CHAR\_SEL >>>  
 24 USB\_CHAR\_CT1 >>>

To Connector

35 USB2\_CHAR\_N <<<  
 35 USB2\_CHAR\_P <<<

To PCH

15 USB2\_USB20\_N <<<  
 15 USB2\_USB20\_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 <sup>(1)</sup>	ILIM_LO	Data Lines Connected
1	1	1	1	CDP <sup>(1)</sup>	ILIM_HI	

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
USB CHARGER		
Size	Document Number	Rev
Custom	Woody/Buzz KBL	-2
Date:	Tuesday, July 25, 2017	Sheet 36 of 106



# Blanking

Count		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>		Sheet <div>37</div> of <div>106</div>

Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Reserved</div>	
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>
Date <div>Tuesday, July 25, 2017</div>	Rev <div>-2</div>
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# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>	Sheet <div>39</div>	of <div>106</div>

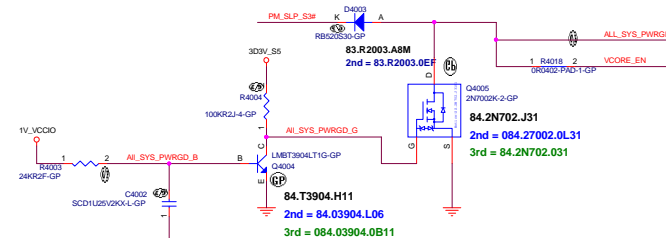
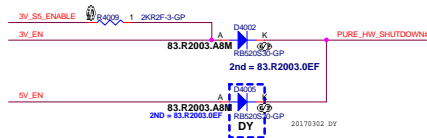
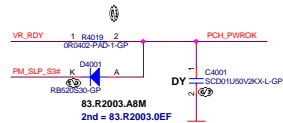
## Power Sequence

26.46 VR\_RDY >>>  
20 PCH\_PWROK <<<  
20.24,40,53.60 PM\_SLP\_S3# >>>  
24 3V\_SS\_ENABLE >>>  
45 3V\_EN <<<  
24.45 5V\_EN <<<  
24.26 PURE\_HW\_SHUTDOWN# >>>  
20.24 ALL\_SYS\_PWRGD <<<  
46 VCORE\_EN <<<

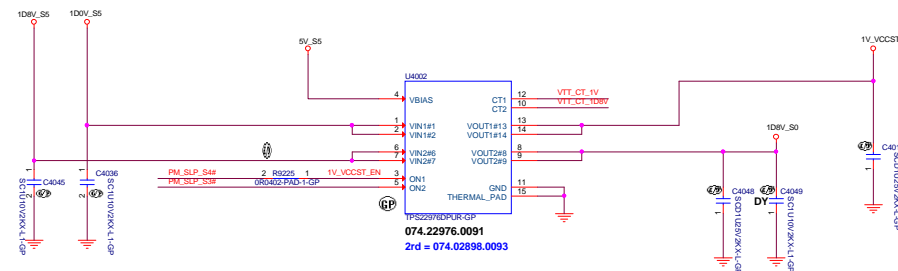
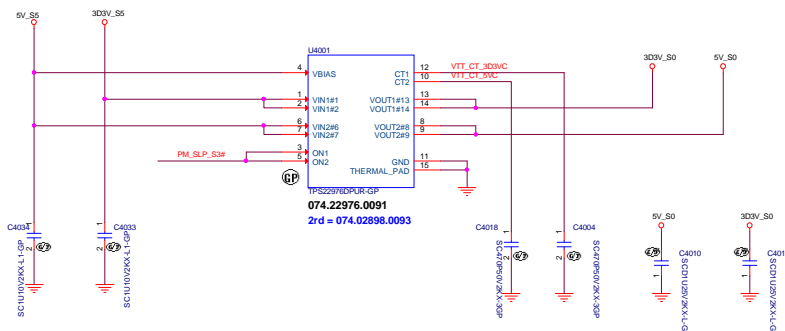
## Run Power

20.24,51 PM\_SLP\_S4# >>>  
20.24,40,53.60 PM\_SLP\_S3# >>>

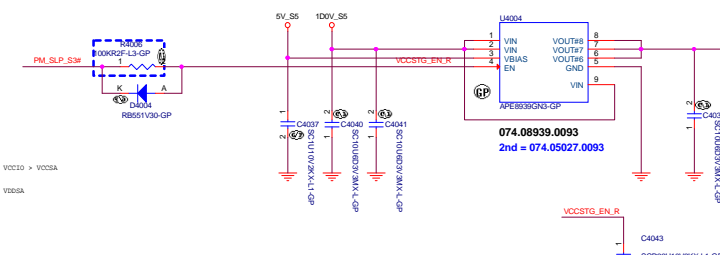
## Power Sequence



## ANNIE Run Power



1126 81mm  
Turning RC for DRAM  
VCCIO = 800mS  
2.5V = SLP\_S4  
VCCIO = 800mS  
Sequence should  
D084 =  
SLP\_S4 > 2.5V > VDDQ > VCCIO > VCCA  
D083 =  
SLP\_S4 > VDDQ > VDDIO > VDDSA  
D084 = 100K  
R4004 = 100K  
C4043 = 0.22u  
D5702 = stuff  
D083 =  
R4004 = 33K  
C4043 = 0.1u  
D5702 = stuff



Count

緯創資通 Wistron Corporation	
2/F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan 301, Taiwan, R.O.C	
Title Power Plane Enable & SEQUENCE	
Size Custom	Woody/Buzz KBL
Date Tuesday, July 25, 2017	Sheet 40 of 106

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Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>		Sheet <div>41</div> of <div>106</div>

Blanking

Count

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**Woody/Buzz KBL**

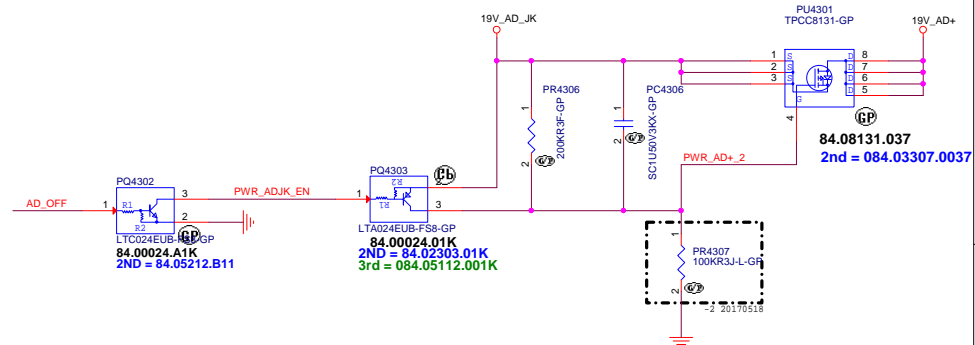
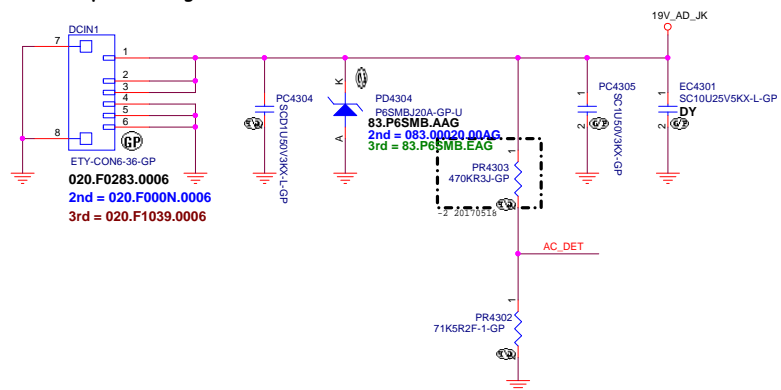
Rev  
**-2**

Date: Tuesday, July 25, 2017

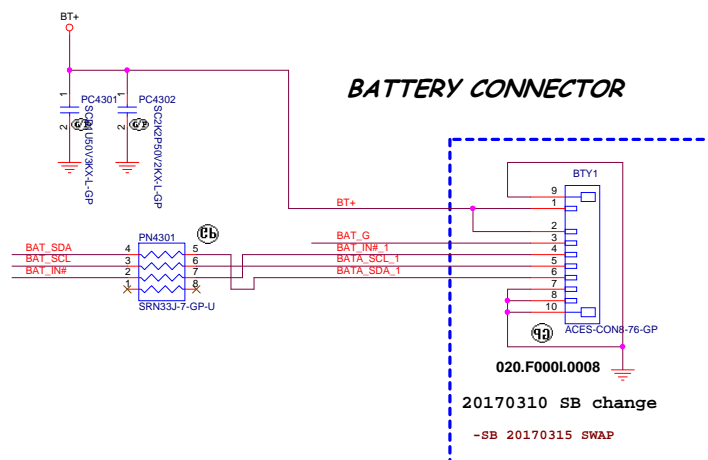
Sheet 42 of 106

# ANNIE solution

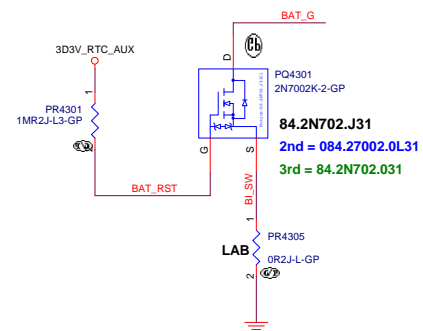
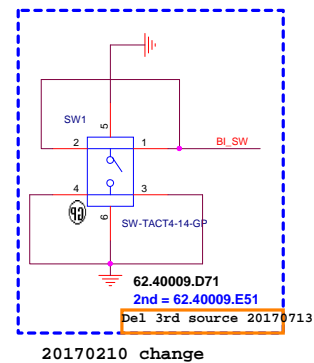
## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR

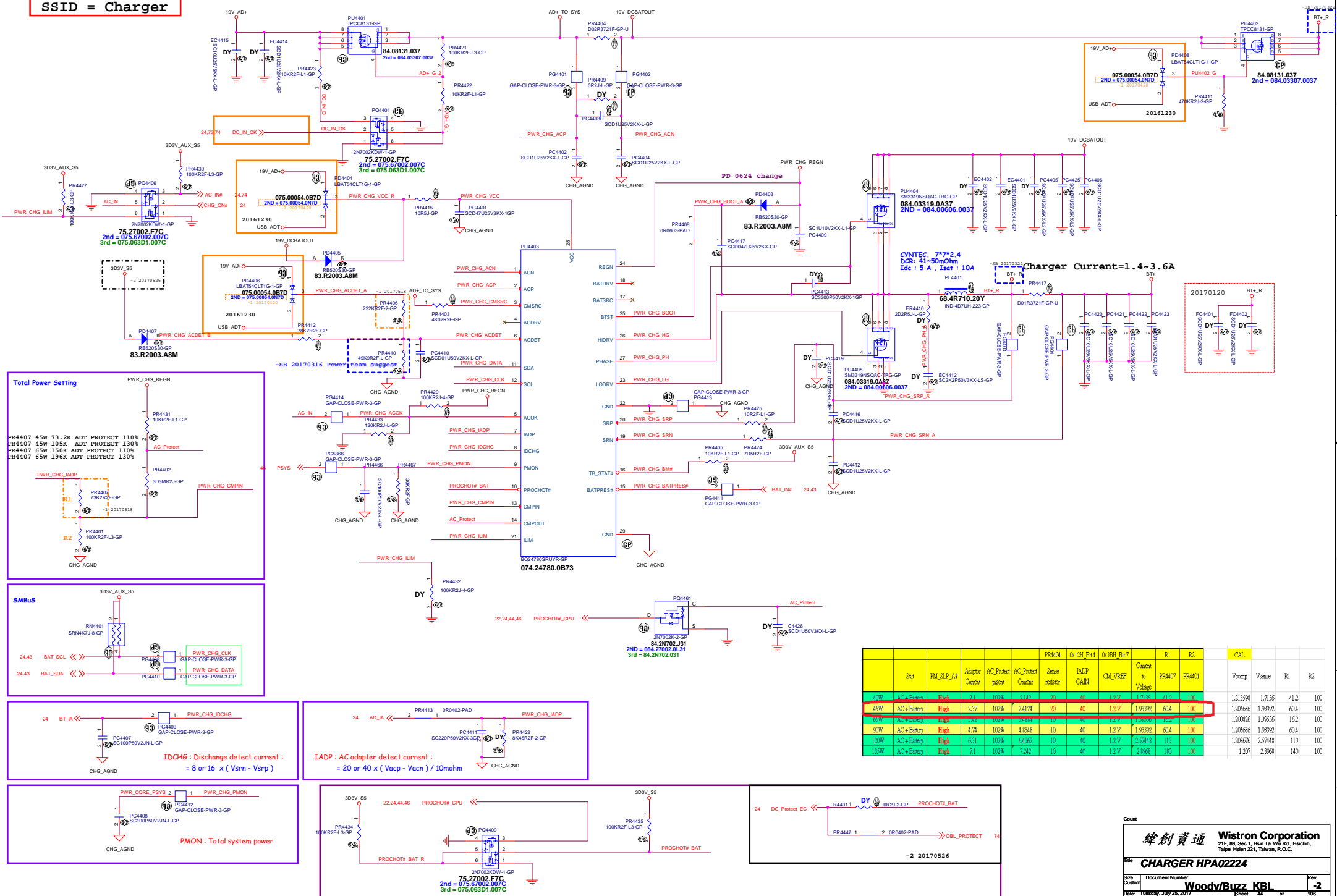


## Battery Insert



Count

SSID = Charger



Count

緯創資通 Wistron Corporation  
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Rev: CHARGER HPA02224

Doc: Document Number

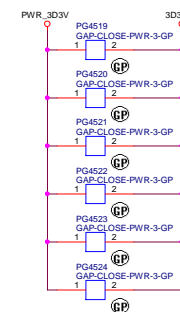
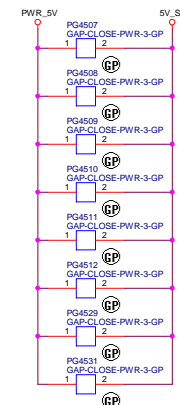
Rev: 2

Woody/Buzz KBL

Date: 1/25/2017, July 26, 2017

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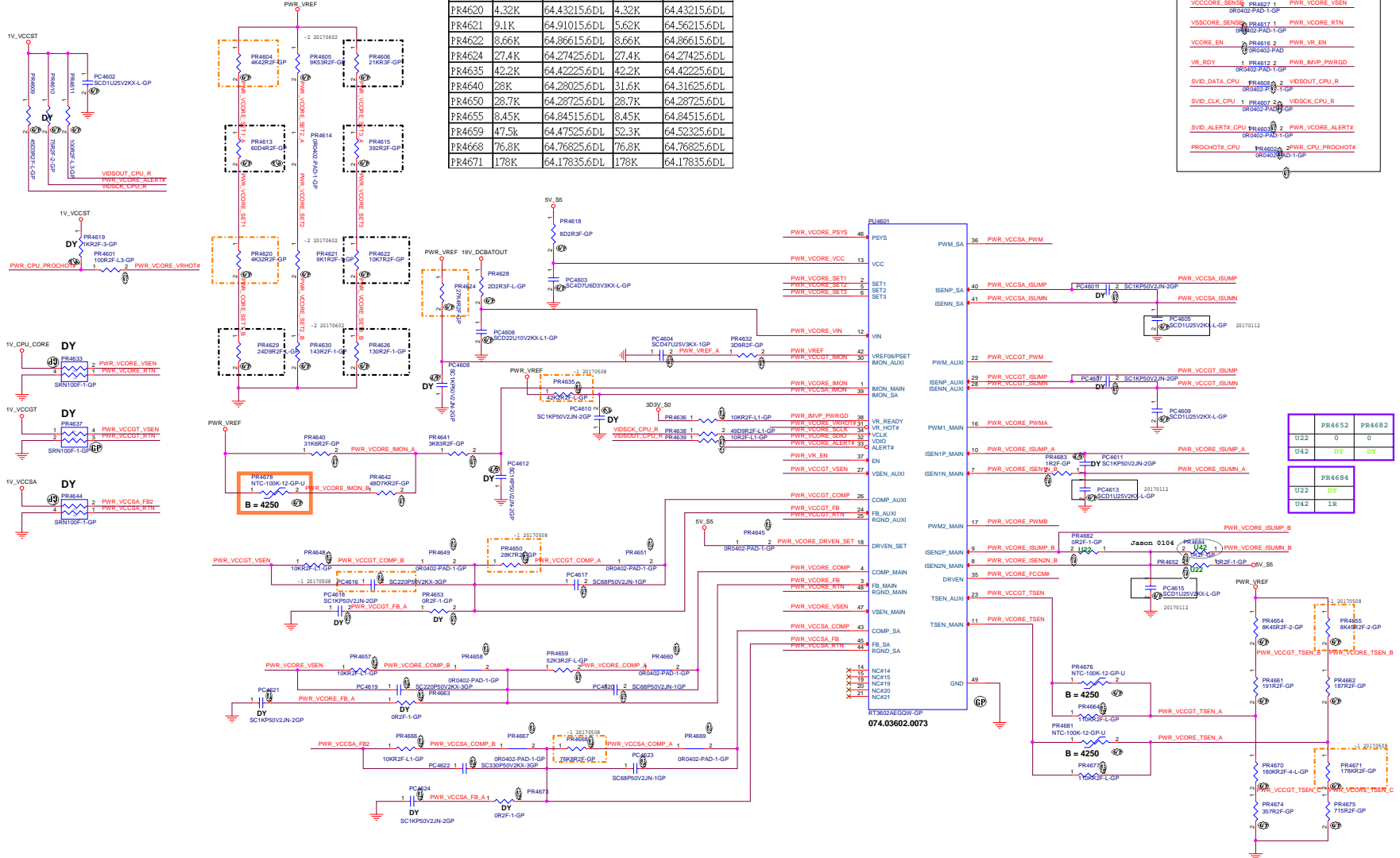
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Title			
<b>RT6226 5V/3D3V</b>			
Size	Document Number	Rev	
Custom	Woody/Buzz_KBL	-2	
Date:	08/08/01, July 25, 2017	Sheet	45 of 108

Main Func = CPU\_CORE

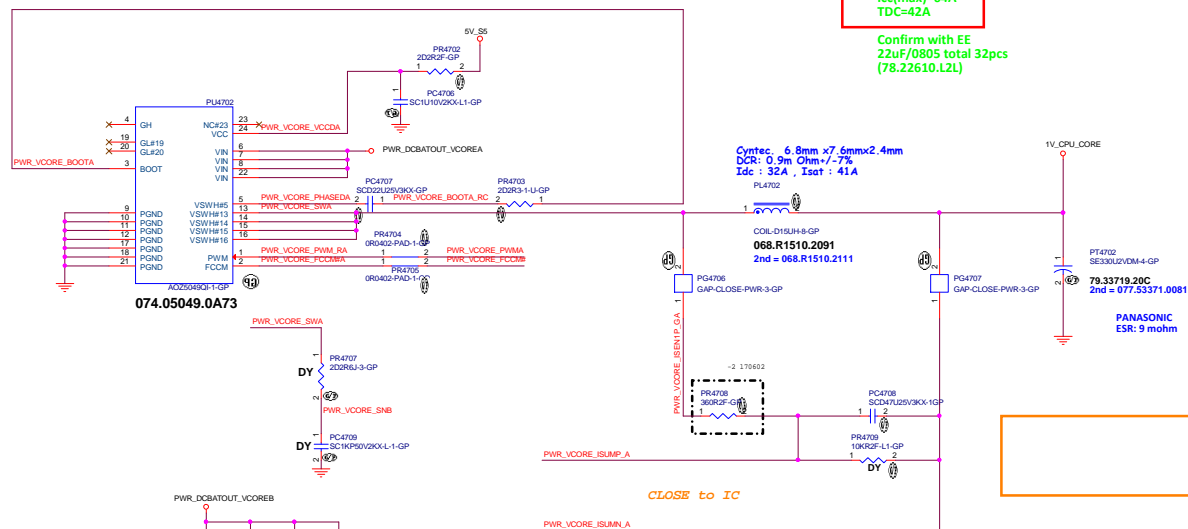
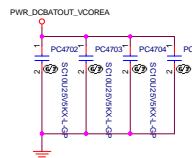
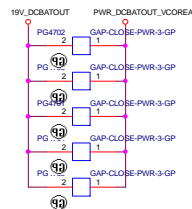
OFFPAGE

BOM control			
Location	U22	U42	U42
PR4604	4.42K	64.44215.6DL	64.44215.6DL
PR4605	9.53K	64.95315.6DL	64.26125.6DL
PR4606	18K	64.18025.55L	64.18025.55L
PR4615	665ohm	64.66505.6DL	665ohm
PR4616	220PF	78.22124.2FL	78.22124.2FL
PR4620	4.32K	64.43215.6DL	64.43215.6DL
PR4621	9.1K	64.91015.6DL	64.56215.6DL
PR4622	8.66K	64.86615.6DL	64.86615.6DL
PR4624	27.4K	64.27425.6DL	64.27425.6DL
PR4635	42.2K	64.42225.6DL	64.42225.6DL
PR4640	28K	64.28025.6DL	64.31625.6DL
PR4650	28.7K	64.28725.6DL	64.28725.6DL
PR4655	8.45K	64.84515.6DL	64.84515.6DL
PR4659	47.5K	64.47525.6DL	64.52325.6DL
PR4668	76.8K	64.76825.6DL	64.76825.6DL
PR4671	1.78K	64.17835.6DL	64.17835.6DL

PSYS	PR4643	2	PWR_VCORE_PSYS
VCCSA_SENSE	PR4631	1	PWR_VCCSA_FB2
VSSA_SENSE	PR4631	1	PWR_VCCSA_RTIN
VSGT_SENSE	PR4631	1	PWR_VCGT_RTIN
VCGT_SENSE	PR4631	1	PWR_VCGT_VSEN
VCCORE_SENSE	PR4627	1	PWR_VCORE_VSEN
VSSCORE_SENSE	PR4617	1	PWR_VCORE_RTIN
VCORE_EN	PR4616	2	PWR_VL_EN
VL_RDY	PR4612	2	PWR_MVP_PWRGD
SVID_DATA_CPU	PR4608	2	VDSOUT_CPU_R
SVID_CLK_CPU	PR4607	2	VDSCK_CPU_R
SVID_ALERTS_CPU	PR4607	2	PWR_VCORE_ALERTS
PROCHOT_CPU	PR4600	1	PWR_CPU_PROCHOT



46	PWR_VCORE_SUMP_A	<<<	_____
46	PWR_VCORE_SUMP_LA	<<<	_____
46	PWR_VCORE_PWMA	>>>	_____
46,48,50	PWR_VCORE_FOCM#	>>>	_____
46	PWR_VCORE_ISUMP_B	<<<	_____
46	PWR_VCORE_ISUMP_LB	<<<	_____
46	PWR_VCORE_PWMB	>>>	_____



SKL\_U42  
Icc(max)=64A  
TDC=42A

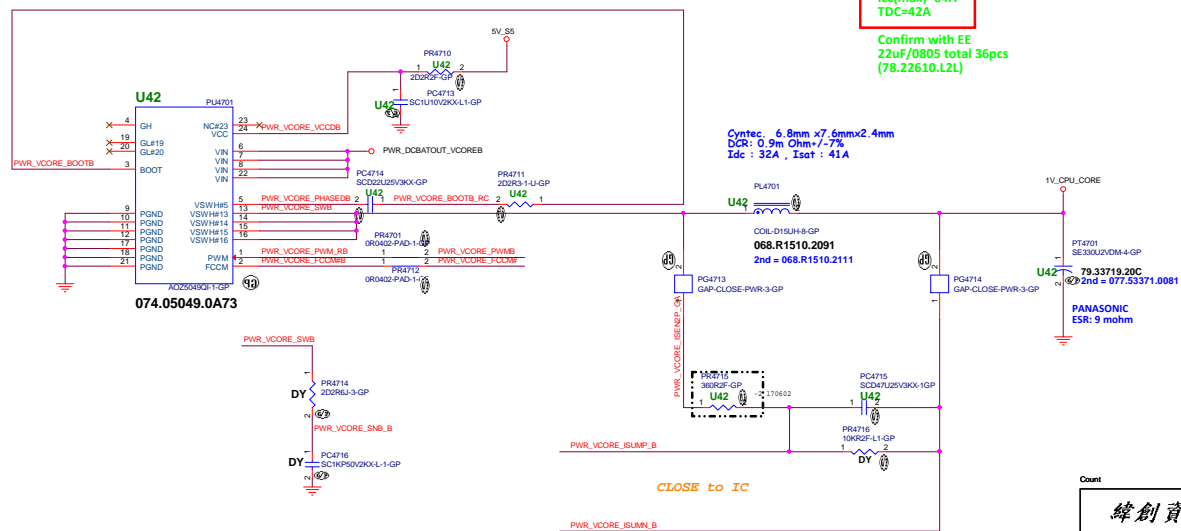
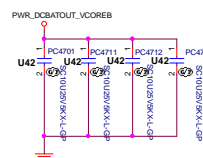
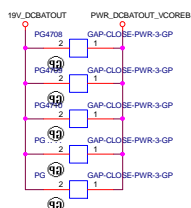
Confirm with EE  
22uF/0805 total 32pcs  
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm  
DCR: 0.9m Ohm+/-7%  
Idc : 32A , Isat : 41A

068.R1510.2091  
2nd = 068.R1510.2111

PT4702  
SE330U2VDM-4-GP  
**79.33719.20C**  
**2nd = 077.53371.0081**

Location	U22		U42	
PR4708	330ohm	64.33005.6DL	287ohm	64.28705.6DL



SKL\_U42  
Icc(max)=64A  
TDC=42A

Confirm with EE  
22uF/0805 total 36pcs  
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm  
DCR: 0.9m Ohm+/-7%  
Idc : 32A , Isat : 41A

2nd = 068.R1510.2111

Count

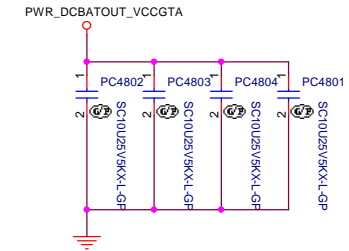
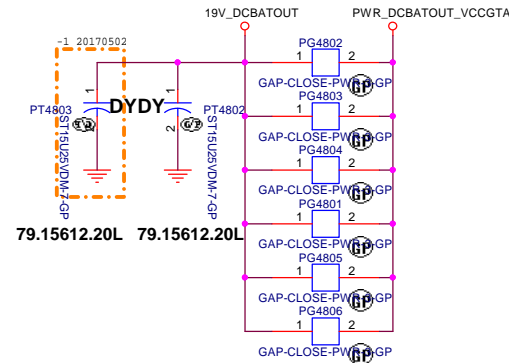
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>CPU VCORE(2/3)</b>
-------	-----------------------

Size Custom	Document Number <b>Woody/Buzz KBL</b>	Rev <b>-2</b>
Date 10/26/2017	Sheet 47 of 106	

Date: Tuesday, July 25, 2017 Sheet 47 of 106

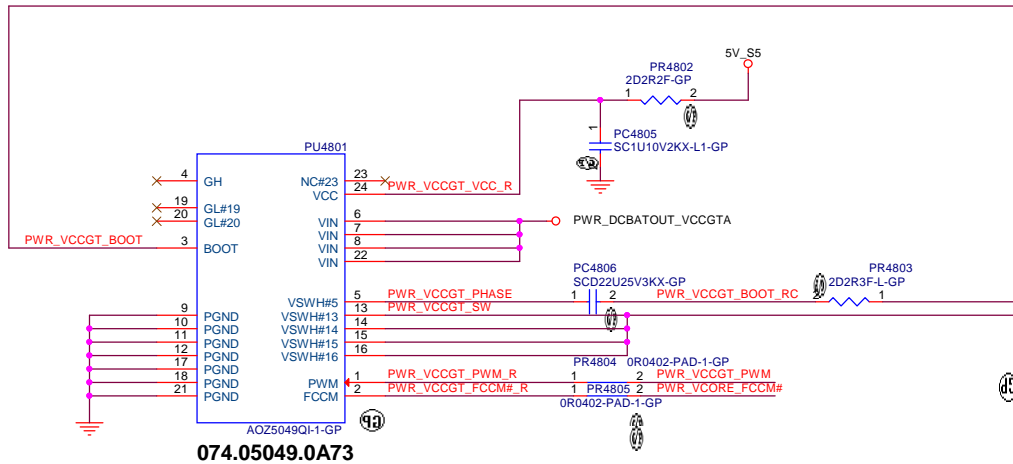
Main Func = CPU\_CORE



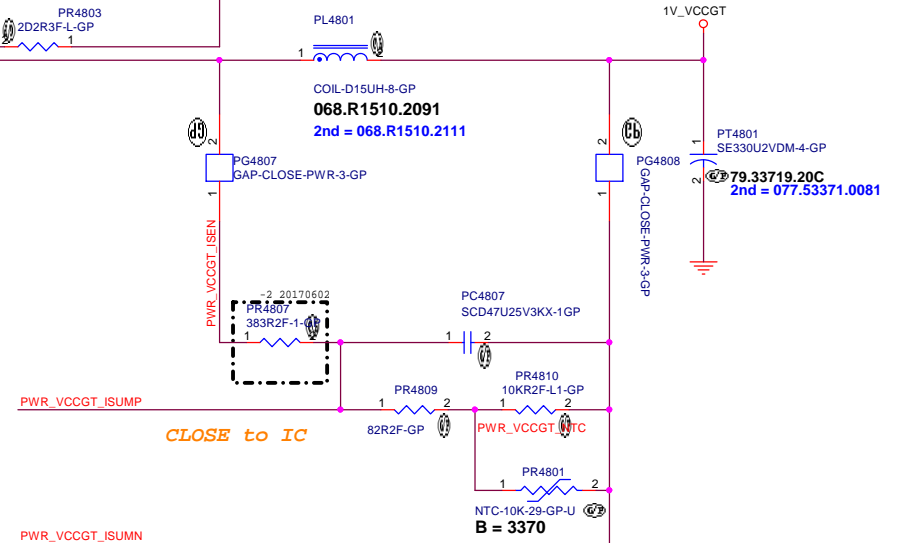
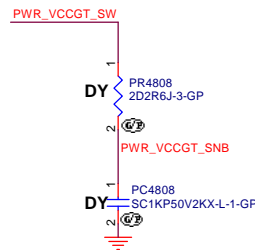
SKL\_U42  
Icc(max)=28A  
TDC=12A

Confirm with EE  
22uF/0805 total 26pcs  
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm  
DCR: 0.9m Ohm+/-7%  
Idc : 32A , Isat : 41A



074.05049.0A73



Location	U22	U42
PR4807	430ohm	64.43005.6DL
		324ohm
		64.32405.6DL

Count

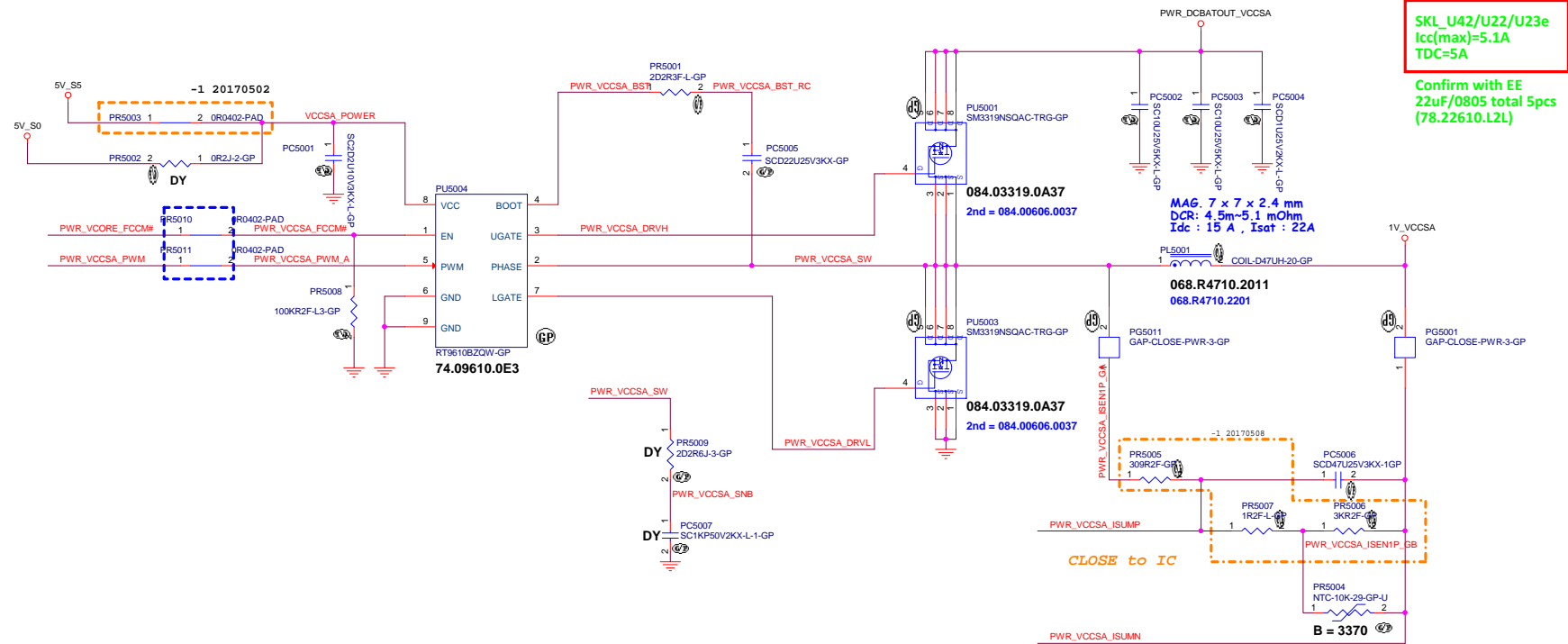
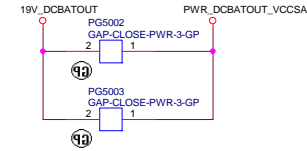
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU VCCGT(3/3)	
Size A3	Document Number
Woody/Buzz KBL	
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# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
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```
Main Func = CPU_CORE
```



SKL\_U42/U22/U23e  
Icc(max)=5.1A  
TDC=5A

Confirm with EE  
22uF/0805 total 5pcs  
(78.22610.L2L)

Count

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
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**VCCSA**

Size
------

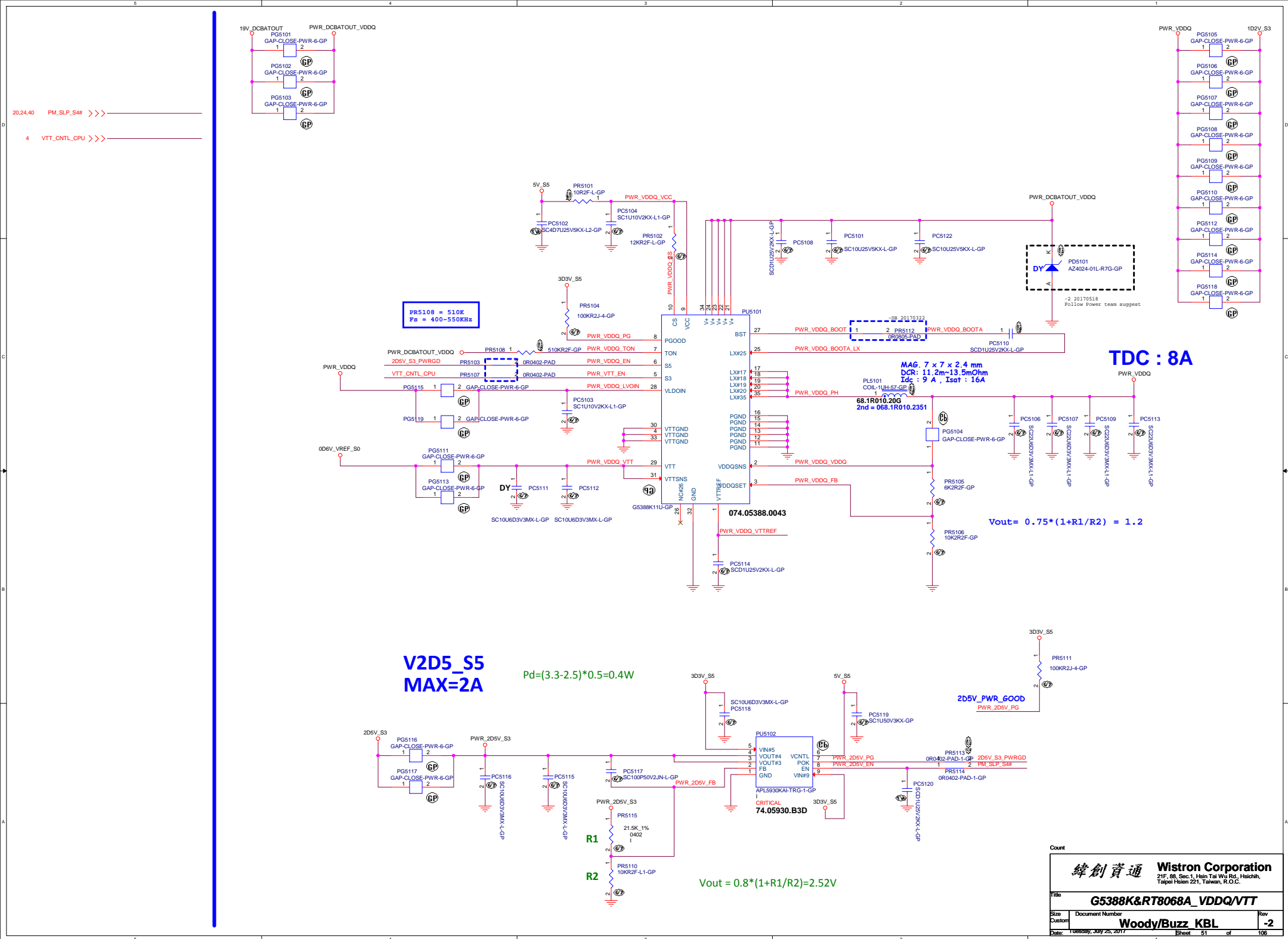
	Document Number
--	-----------------

**Woody/Buzz\_KBL**

rev

Date: Tuesday, July 25, 2017

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53 1D8V\_S5\_PWRGD >>

PR5108 = 510K  
Fs = 400-550KHz

TDC : 3.5A

MAG. 7 x 7 x 2.4 mm  
DCR: 11.2m~13.5mOhm  
Idc : 9 A , Isat : 16A

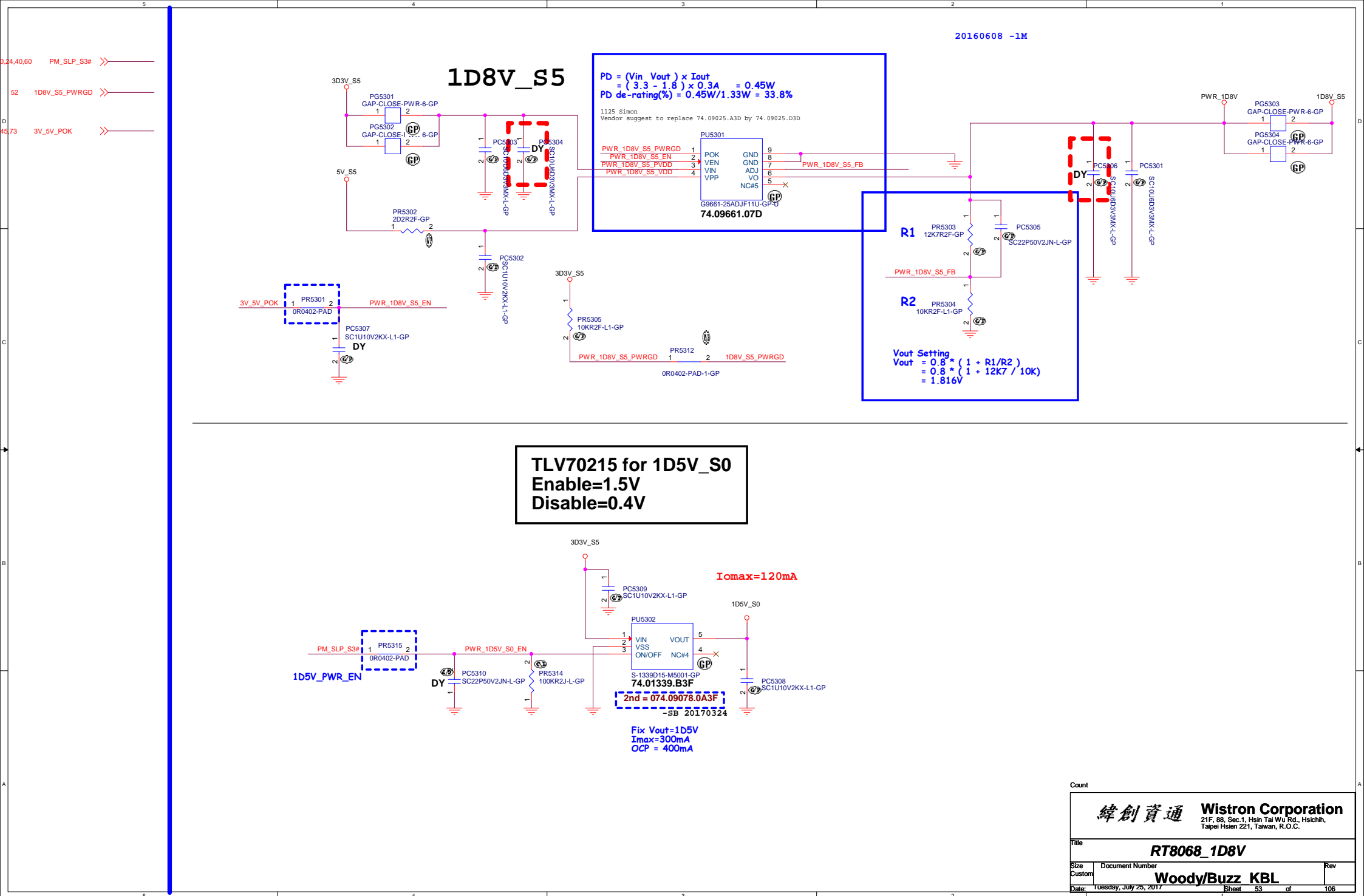
$V_{out} = 0.75 * (1 + R1/R2) = 1.0V$

074.05388.0043

Count


緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

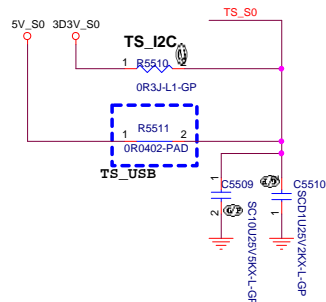
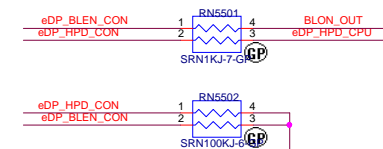
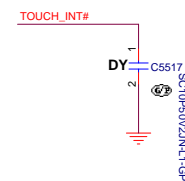
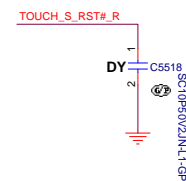
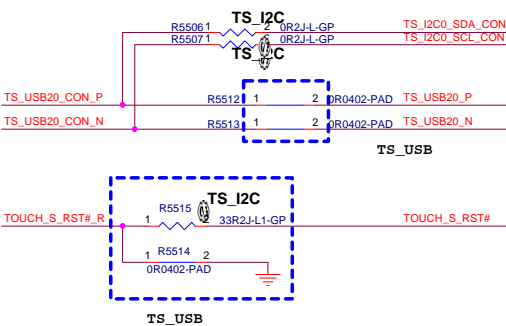
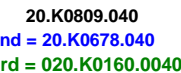
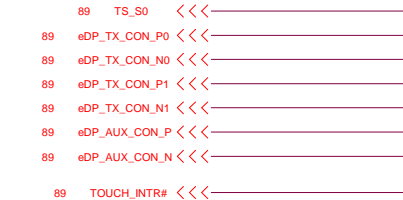
Title			G5388K 1D0V
Size	Document Number	Rev	
A3	Woody/Buzz KBL	-2	
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# Blanking

Count

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>Woody/Buzz_KBL</b>		Rev <b>-2</b>
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Count

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>Woody/Buzz_KBL</b>		Rev <b>-2</b>
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HDMI CONN

```

3      HDMI_DATA_CPU_P0      >>>>>
3      HDMI_DATA_CPU_N0      >>>>>
3      HDMI_DATA_CPU_P1      >>>>>
3      HDMI_DATA_CPU_N1      >>>>>
3      HDMI_DATA_CPU_P2      >>>>>
3      HDMI_DATA_CPU_N2      >>>>>
3      HDMI_DATA_CPU_P3      >>>>>
3      HDMI_DATA_CPU_N3      >>>>>

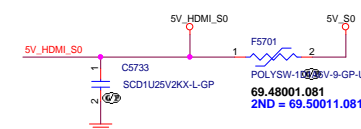
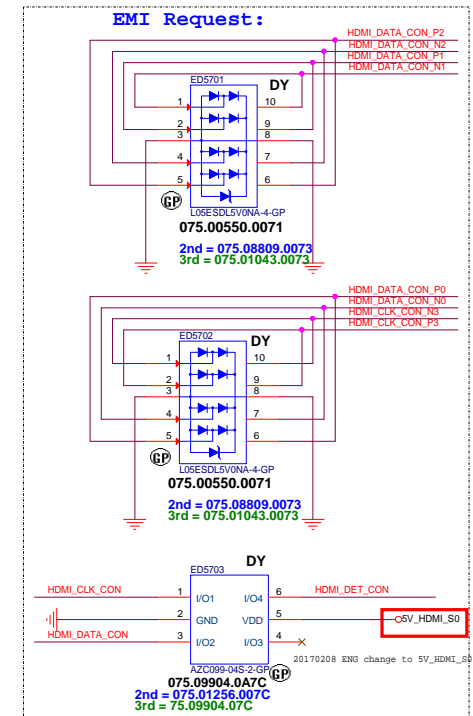
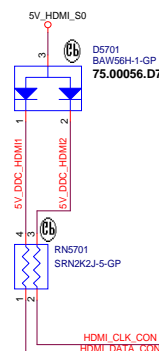
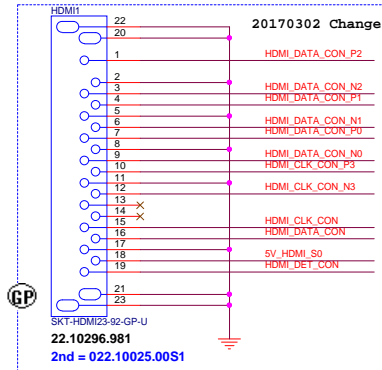
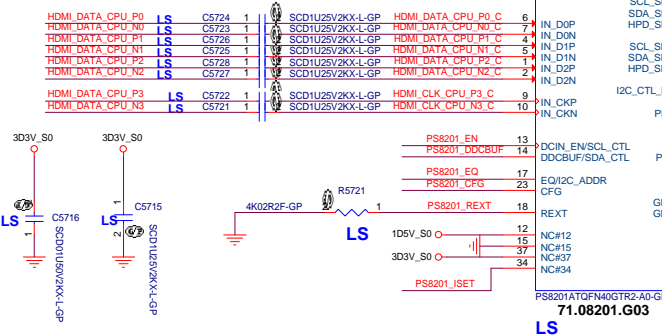
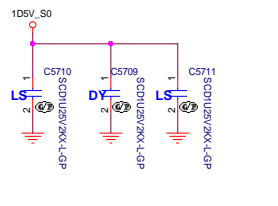
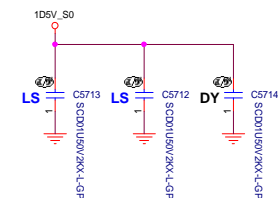
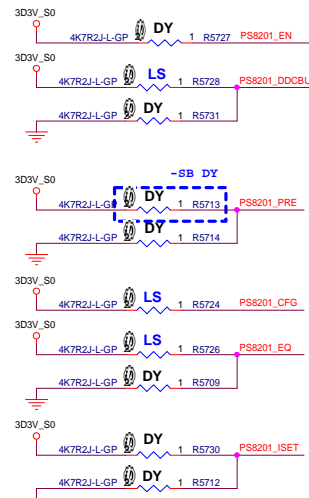
314    HDMI_CLK_CPU          >>>>>
314    HDMI_DATA_CPU         >>>>>
3      HDMI_DET_CPU          >>>>>

89     HDMI_CLK_CON_N3       <<<<<
89     HDMI_CLK_CON_P3       <<<<<

89     HDMI_DATA_CON_P0      <<<<<
89     HDMI_DATA_CON_N0      <<<<<
89     HDMI_DATA_CON_P1      <<<<<
89     HDMI_DATA_CON_N1      <<<<<
89     HDMI_DATA_CON_P2      <<<<<
89     HDMI_DATA_CON_N2      <<<<<

89     HDMI_CLK_CON          <<<<<
89     HDMI_DATA_CON         <<<<<
89     HDMI_DET_CON          <<<<<

```



Count			
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Heishih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>HDMI Level Shift/Connector</b>			
Size	Document Number		Rev <b>-2</b>
<b>Woody/Buzz KBL</b>			
Date:	Tuesday, July 25, 2017	Sheet 57	of 106

Blanking

Count

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A	Document Number		Rev
	Woody/Buzz KBL		-2
Date:	Tuesday, July 25, 2017	Sheet	58 of 106

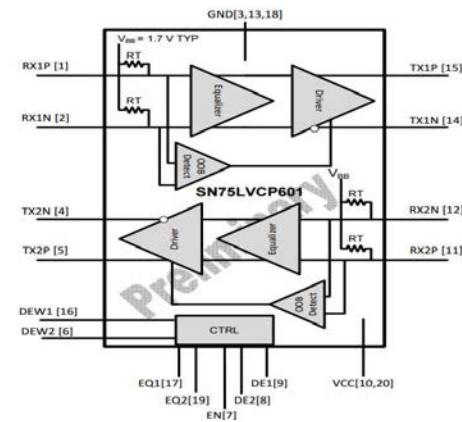
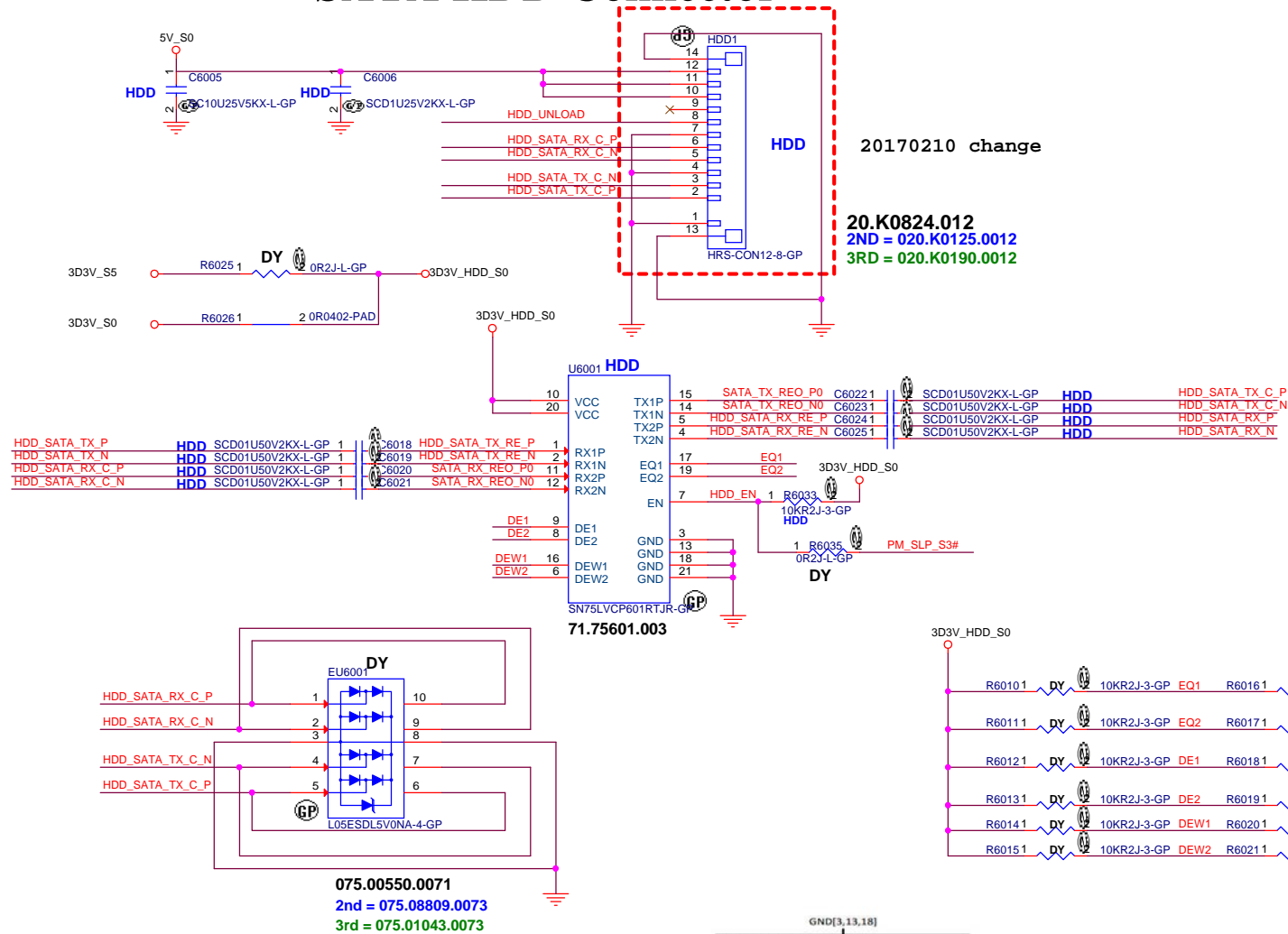


# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>DVI(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz_KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>		Sheet <div>59</div> of <div>106</div>

## SATA HDD Connector



Count

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
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## HDD GSENSOR

Size	Custom
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Document Number
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**Woody/Buzz KBL**

Rev

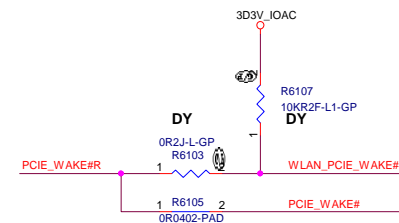
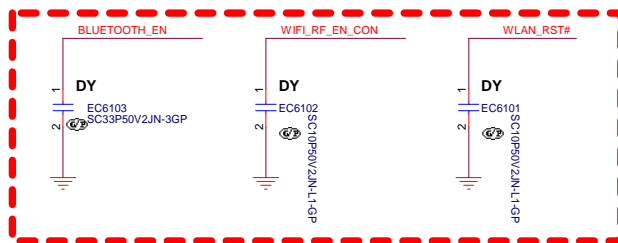
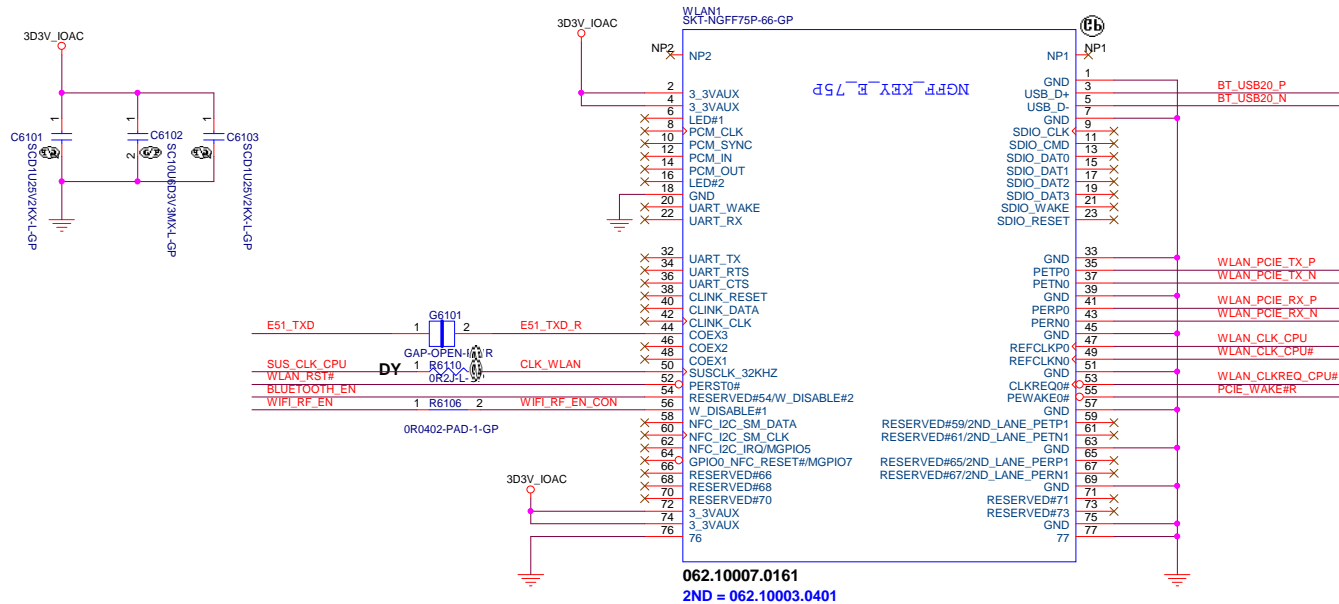
**-2**

Date: Tuesday, July 25, 2017

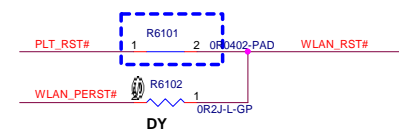
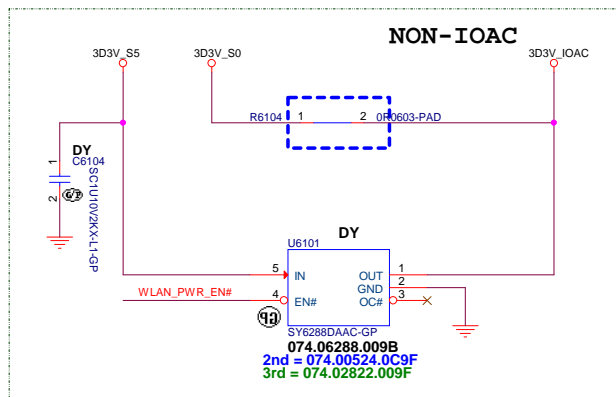
Sheet 60 of 106

# SSID = Wireless Mini Card Connector(802.11a/b/g/n)

24,68	E51_TXD >>>
24,89	BLUETOOTH_EN >>>
24	WIFI_RF_EN <<<
20,24,62,68,89,91	PLT_RST# >>>
24	WLAN_PERST# >>>
15,89	WLAN_PCIE_TX_P >>>
15,89	WLAN_PCIE_TX_N >>>
15,89	WLAN_PCIE_RX_P >>>
15,89	WLAN_PCIE_RX_N >>>
16,89	WLAN_CLK_CPU# >>>
16,89	WLAN_CLK_CPU# >>>
24	WLAN_PCIE_WAKE# <<<
20,24,62	PCIE_WAKE# <<<
24	WLAN_PWR_EN# >>>
89	PCIE_WAKE#R <<<
16,89	WLAN_CLKREQ_CPU# <<<
89	WLAN_RST# <<<
89	WIFI_RF_EN_CON <<<
16	SUS_CLK_CPU >>>
15,89	BT_USB20_P >>>
15,89	BT_USB20_N >>>



## NON-IOAC




Count		
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Mini Card-WLAN		
Size Custom	Document Number Woody/Buzz_KBL	Rev -2
Date: Tuesday, July 25, 2017	Sheet 61	of 106

### *Mini Card Connector(mSATA)*

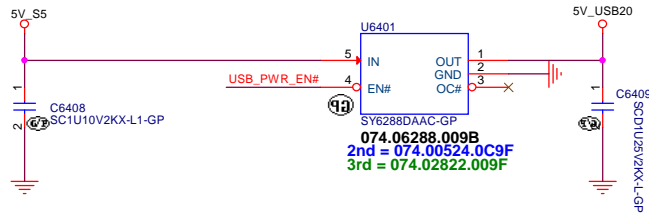
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Count

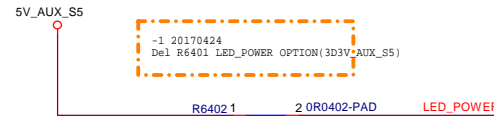
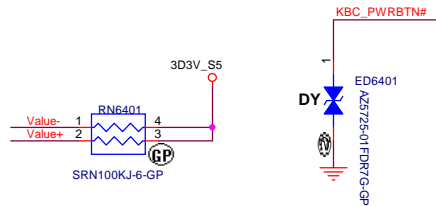
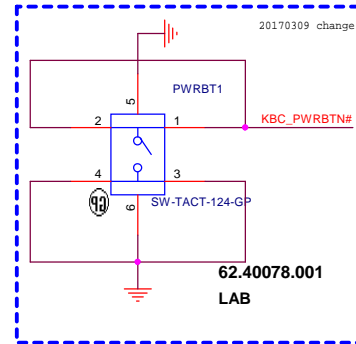
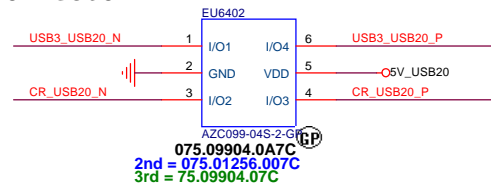
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>Woody/Buzz_KBL</b>		Rev <b>-2</b>
Date: Tuesday, July 25, 2017		Sheet 63 of	106

# SSID = User.Interface

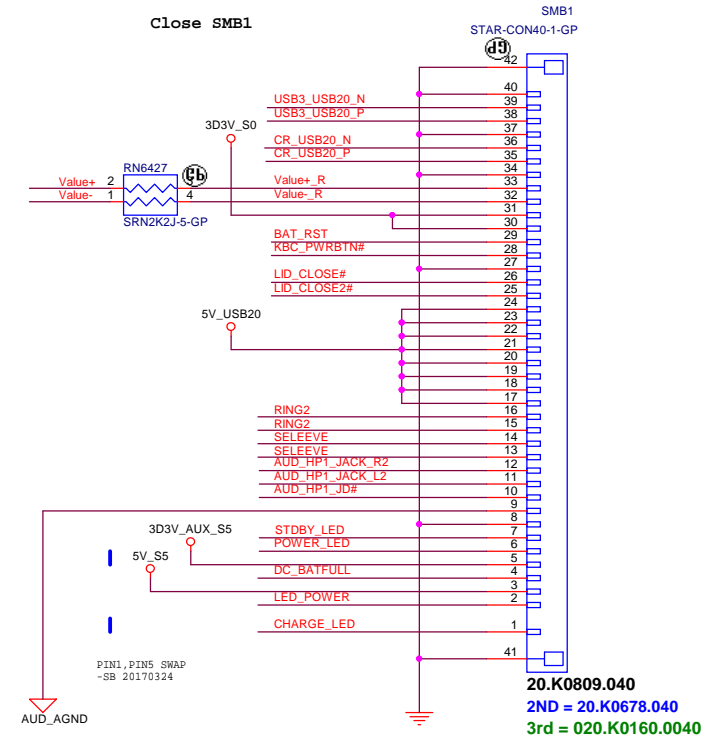
## Low Active 2A



## Close connector



## Close SMB1

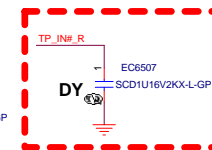
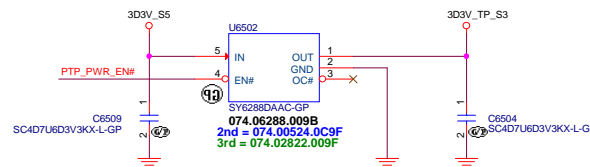
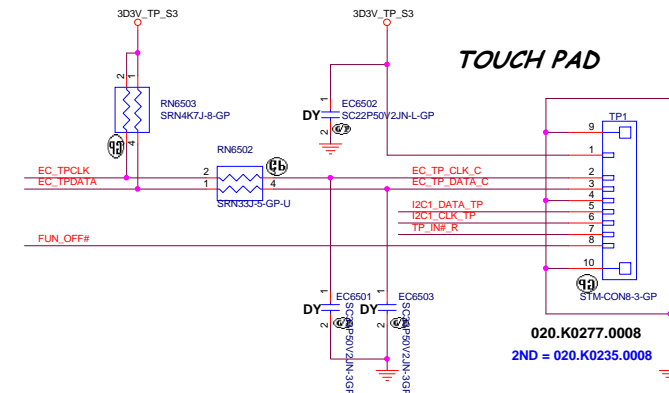
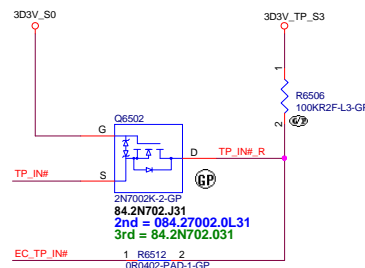
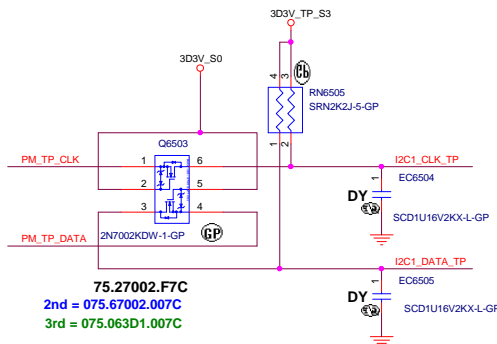


## Count

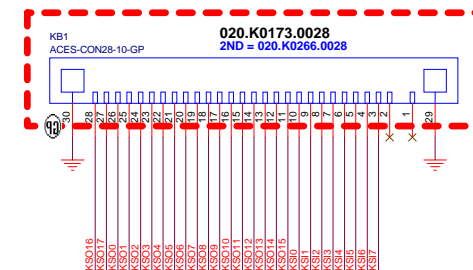
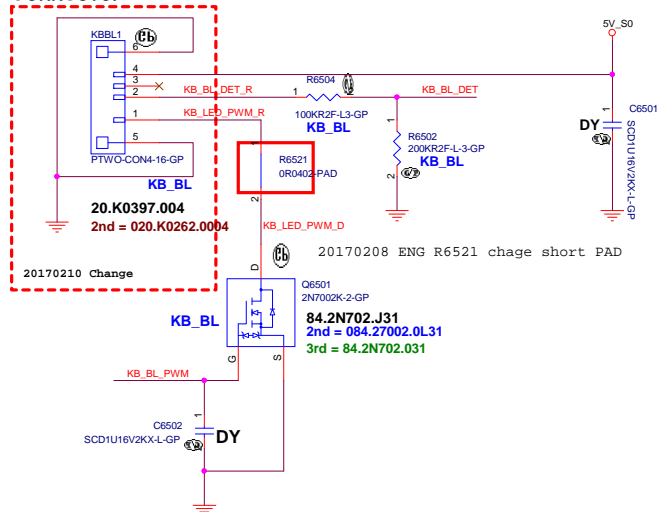
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>LED Bard/Power Button</b>	
Size Custom	Document Number
<b>Woody/Buzz KBL</b>	
Date: Tuesday, July 25, 2017	Sheet 64 of 106
Rev <b>-2</b>	

SSID = KBC

24,89 KSI[0..7] >>> \_\_\_\_\_  
24,89 KSO[0..17] <<< \_\_\_\_\_  
24 EC\_TPCLK << \_\_\_\_\_  
24 EC\_TPDATA << \_\_\_\_\_  
24,89 FUN\_OFF# >>> \_\_\_\_\_  
24 PTP\_PWR\_EN# >>> \_\_\_\_\_  
22 TP\_IN# <<< \_\_\_\_\_  
24 EC\_TP\_IN# <<< \_\_\_\_\_  
6 PM\_TP\_CLK << \_\_\_\_\_  
6 PM\_TP\_DATA << \_\_\_\_\_  
24 KB\_BL\_PWM >>> \_\_\_\_\_  
24 KB\_BL\_DET <<< \_\_\_\_\_  
89 EC\_TP\_CLK\_C << \_\_\_\_\_  
89 EC\_TP\_DATA\_C << \_\_\_\_\_  
89 I2C1\_DATA\_TP << \_\_\_\_\_  
89 I2C1\_CLK\_TP << \_\_\_\_\_  
89 TP\_IN#\_R << \_\_\_\_\_



## Internal Keyboard Connector



1	NC	2	NC	3	C08	4	C07	5	C06	6	C05	7	C04	8	C03	9	C02	10	C01	11	R16	12	R15	13	R14	14	R13	15	R12	16	R11	17	R10	18	R09	19	R08	20	R07	21	R06	22	R05	23	R04	24	R03	25	R02	26	R01	27	R18	28	R17
---	----	---	----	---	-----	---	-----	---	-----	---	-----	---	-----	---	-----	---	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----

C08	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
C07	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
C06	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
C05	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
C04	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
C03	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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C01	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

Count

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.			
Key Board/Touch Pad			
Size	Document Number	Rev	
Custom	Woody/Buzz_KBL	-2	
Date:	Tuesday, July 25, 2017	Sheet	65 of 106



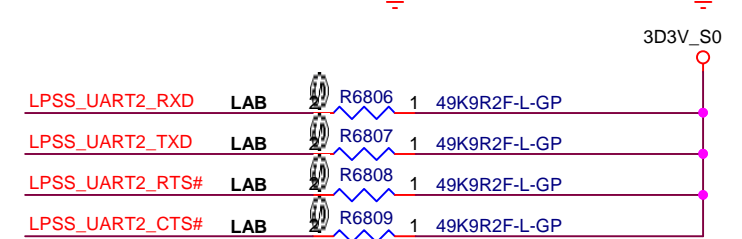
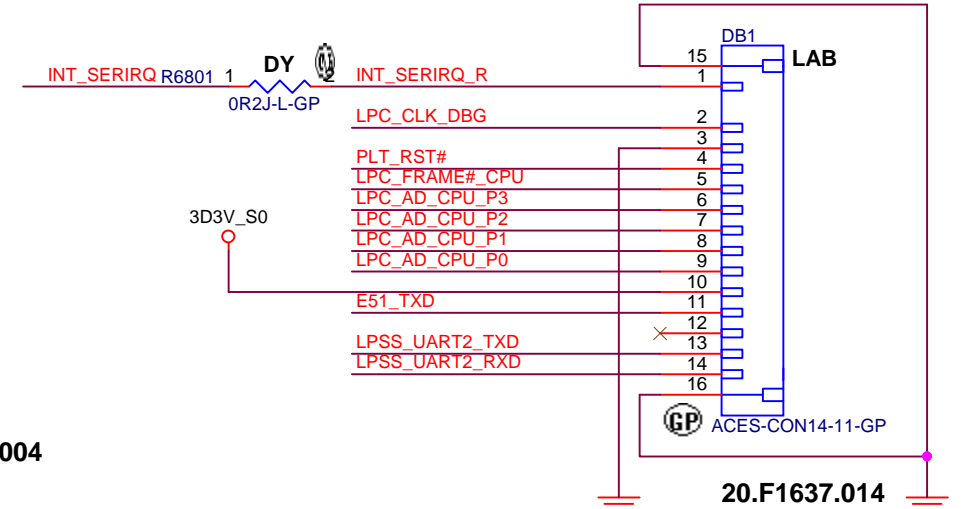
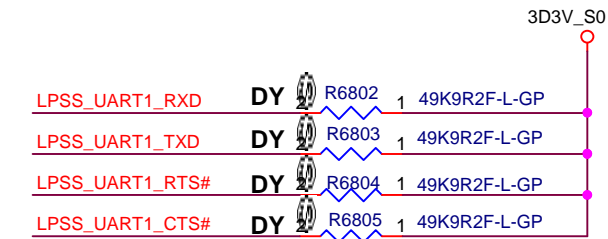
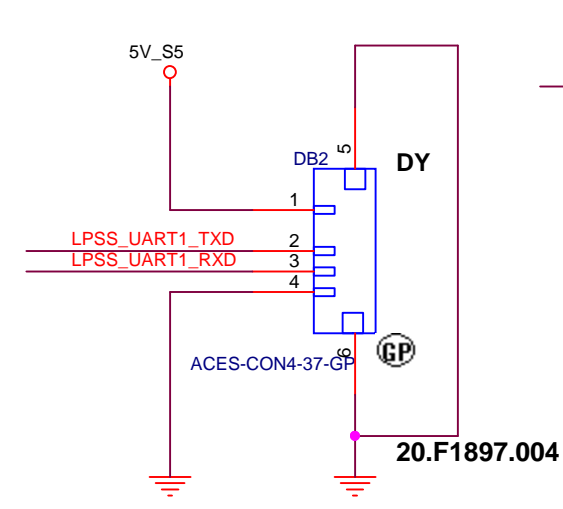
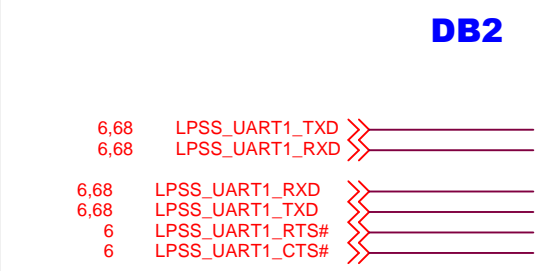
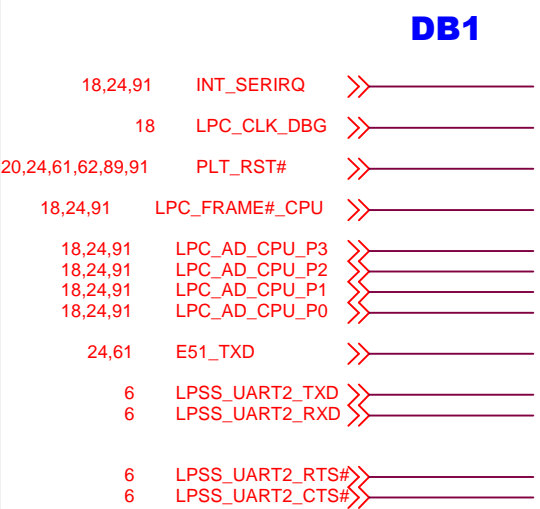
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Count		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	Woody/Buzz KBL	-2
Date:	Tuesday, July 25, 2017	Sheet 66 of 106

# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>		Sheet <div>67</div> of <div>106</div>



Count

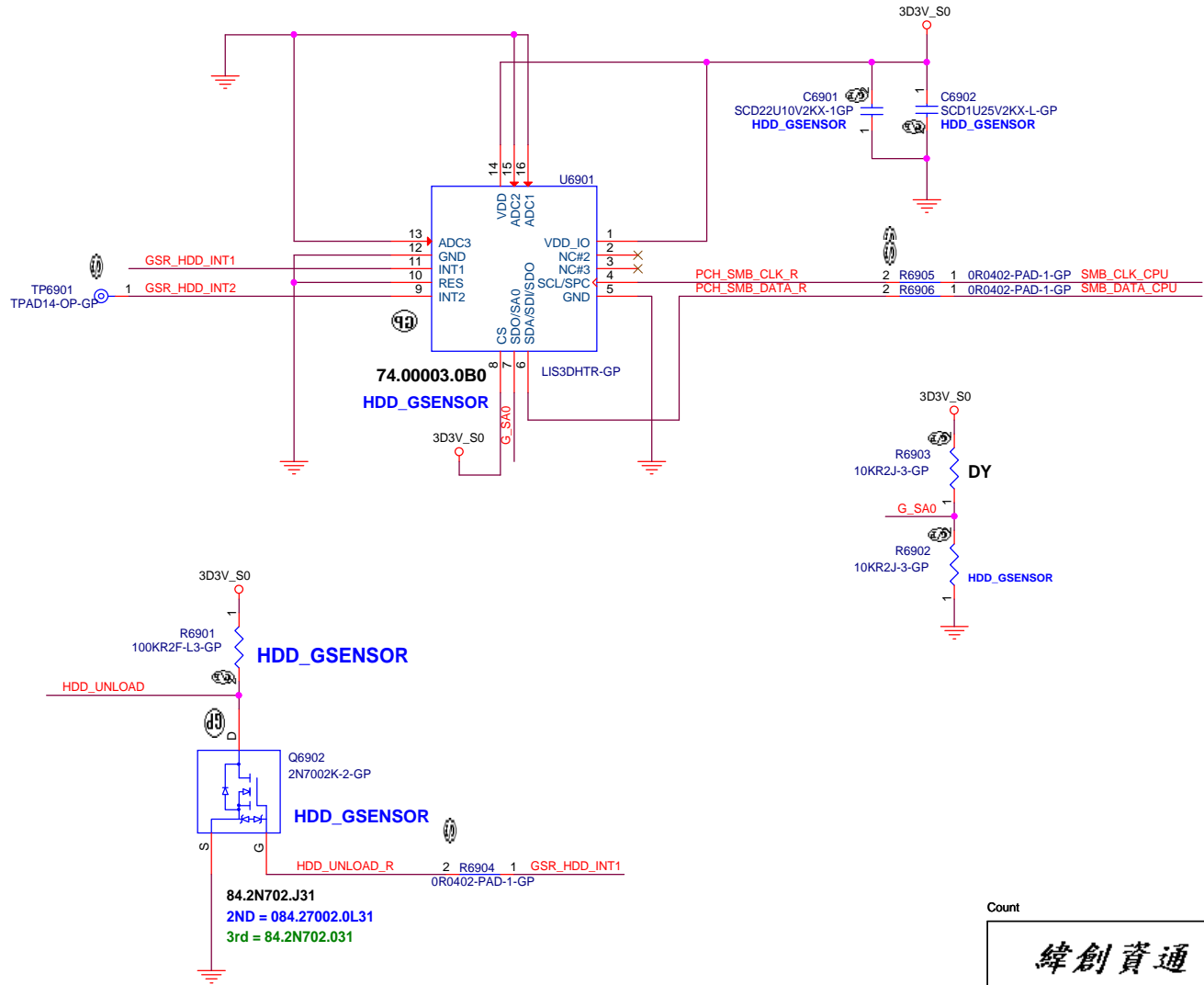
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **Dubug connector**

Size Custom	Document Number	Rev -2
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Woody/Buzz KBL

18 SMB\_CLK\_CPU <<<<  
18 SMB\_DATA\_CPU <<<<  
  
22 GSR\_HDD\_INT1 <<<  
  
60 HDD\_UNLOAD <<<



Count	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD_G_Sensor	
Size Custom	Document Number Woody/Buzz_KBL
Date: Tuesday, July 25, 2017	Rev -2
Sheet 69 of 106	

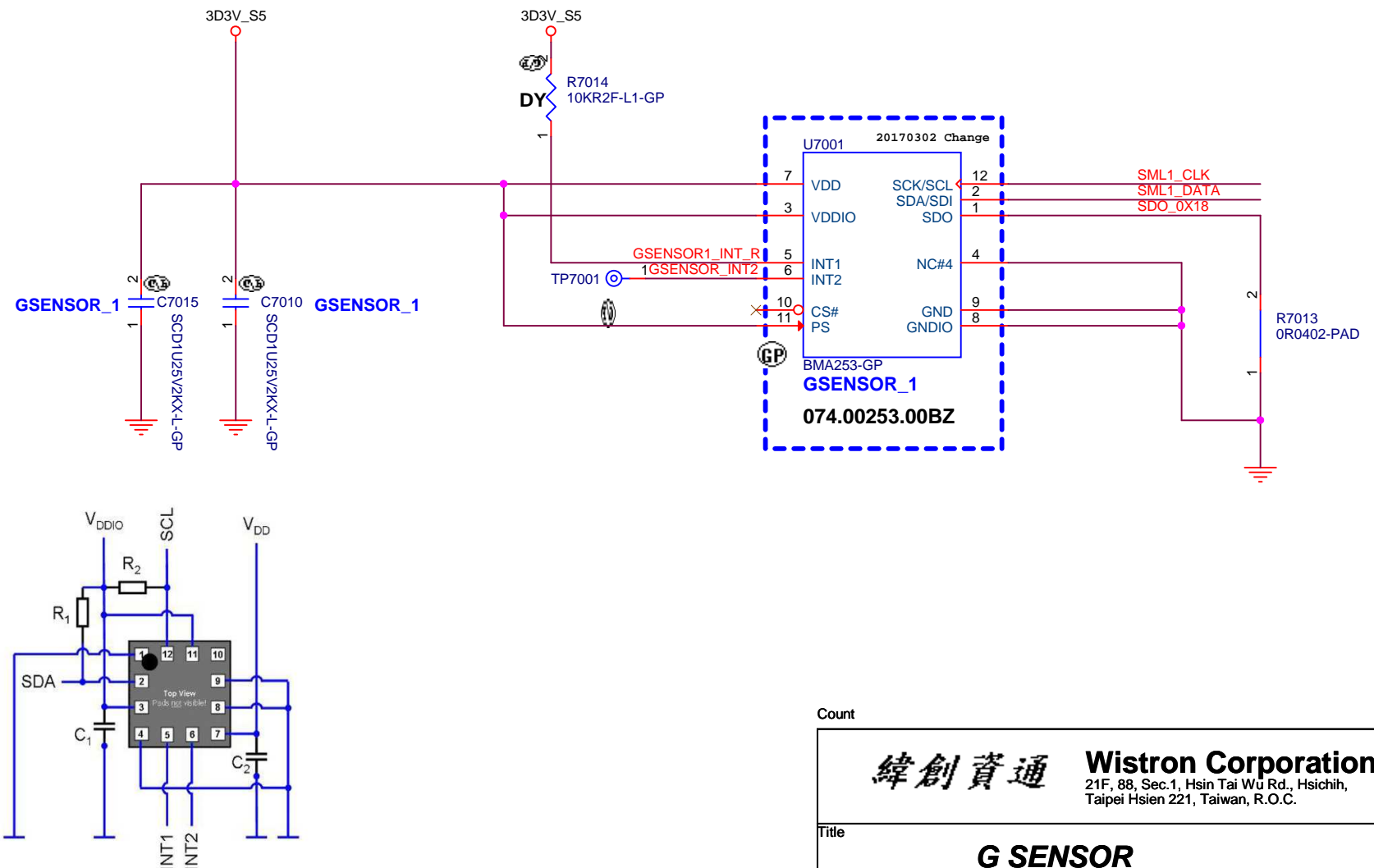
# Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

## SSID = User.Interface

### G Sensor

The default I<sup>2</sup>C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V<sub>DDIO</sub>'.



Count

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**G SENSOR**

Size Document Number

Custom

**Woody/Buzz KBL**

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>	Sheet <div>71</div>	of <div>106</div>

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Count		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Reserved		
Size	Document Number	Rev
A4	Woody/Buzz KBL	-2
Date:	Tuesday, July 25, 2017	Sheet 72 of 106








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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>	Sheet <div>75</div>	of <div>106</div>

# Blanking

Count

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU_PEG(Reserved)</b>			
Size	Project Name		Rev
	<b>Woody/Buzz_KBL</b>		<b>-2</b>
Date: Tuesday, July 25, 2017		Sheet 76	of 106

# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>GPU_DIGITALOUT(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz KBL</div>	Rev <div>-2</div>
Date: Tuesday, July 25, 2017		Sheet 77 of 106

# Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size	Project Name <div>Woody/Buzz_KBL</div>	Rev <div>-2</div>
Date: Tuesday, July 25, 2017		Sheet 78 of 106

# Blanking

Count

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU_GPIO/STRAP(Reserved)</b>			
Size	Project Name		Rev
	<b>Woody/Buzz_KBL</b>		<b>-2</b>
Date:	Tuesday, July 25, 2017	Sheet 79 of	106

Blanking

Count

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>GPU_POWER/GND(Reserved)</div>		
Size	Project Name <div>Woody/Buzz_KBL</div>	Rev <div>-2</div>
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Title <div>Reserved</div>		
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>GPU-VRAM3,4(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Woody/Buzz_KBL</div>	Rev <div>-2</div>
Date <div>Tuesday, July 25, 2017</div>	Sheet <div>82</div>	of <div>106</div>

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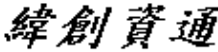
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GPU-VRAM5,6(Reserved)			
Size A4	Document Number Woody/Buzz_KBL		Rev -2
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GPU-VRAM7,8(Reserved)		
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Title <b>VGA_CORE(Reserved)</b>			
Size A4	Document Number <b>Woody/Buzz_KBL</b>		Rev
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Title <div>DIS VGA POWER(Reserved)</div>		
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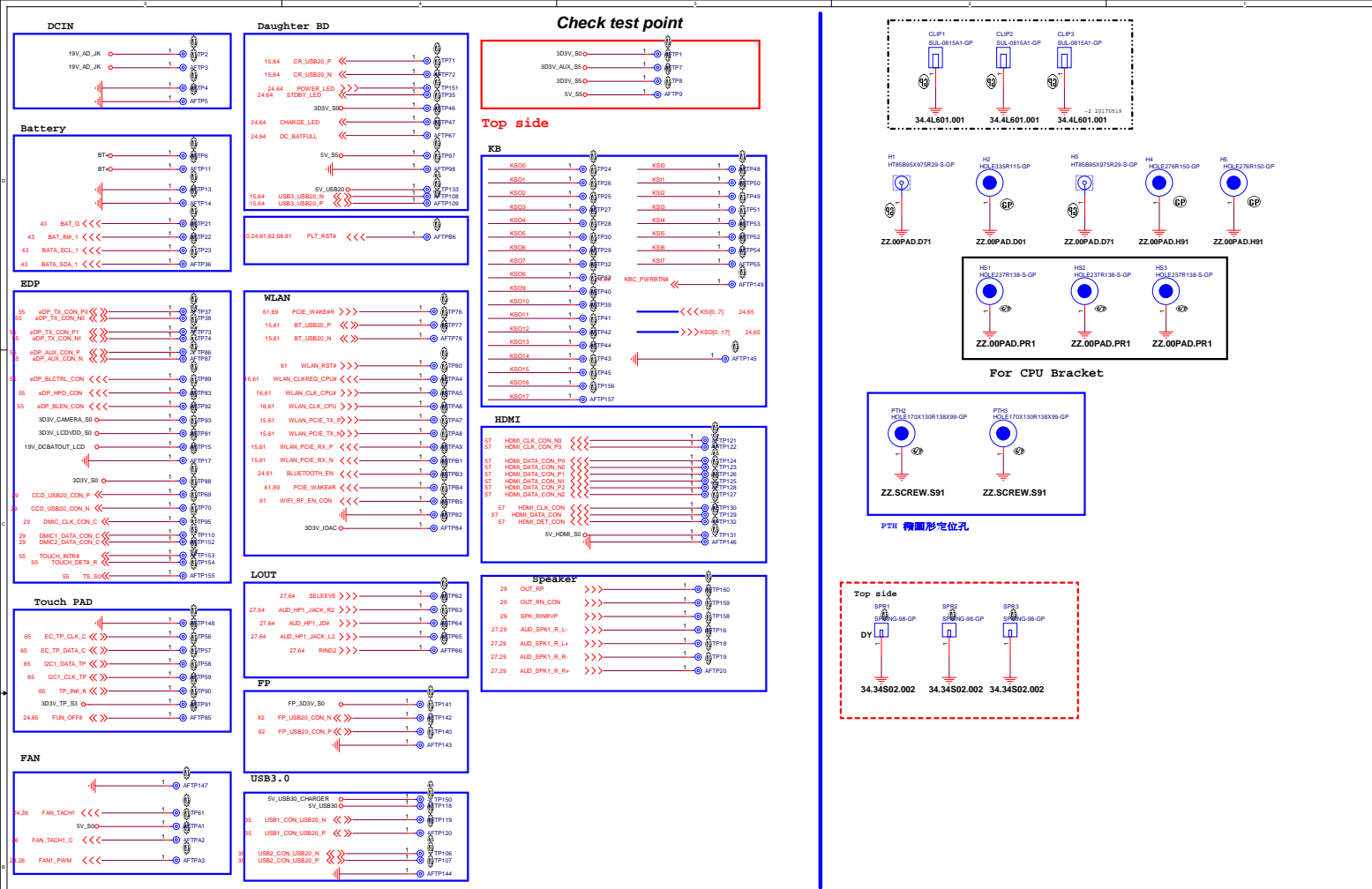
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Title

**NFC(Reserved)**

Size  
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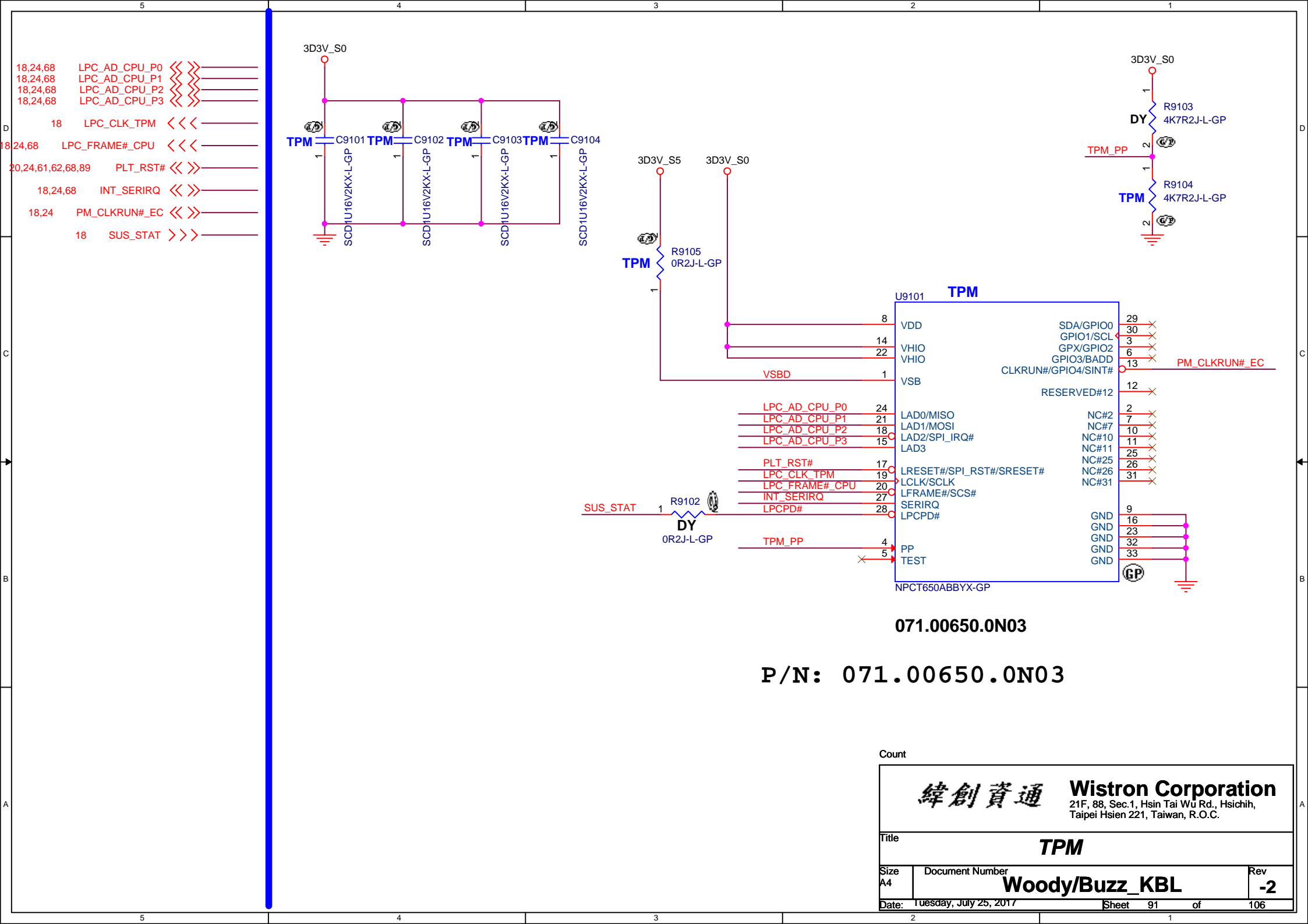
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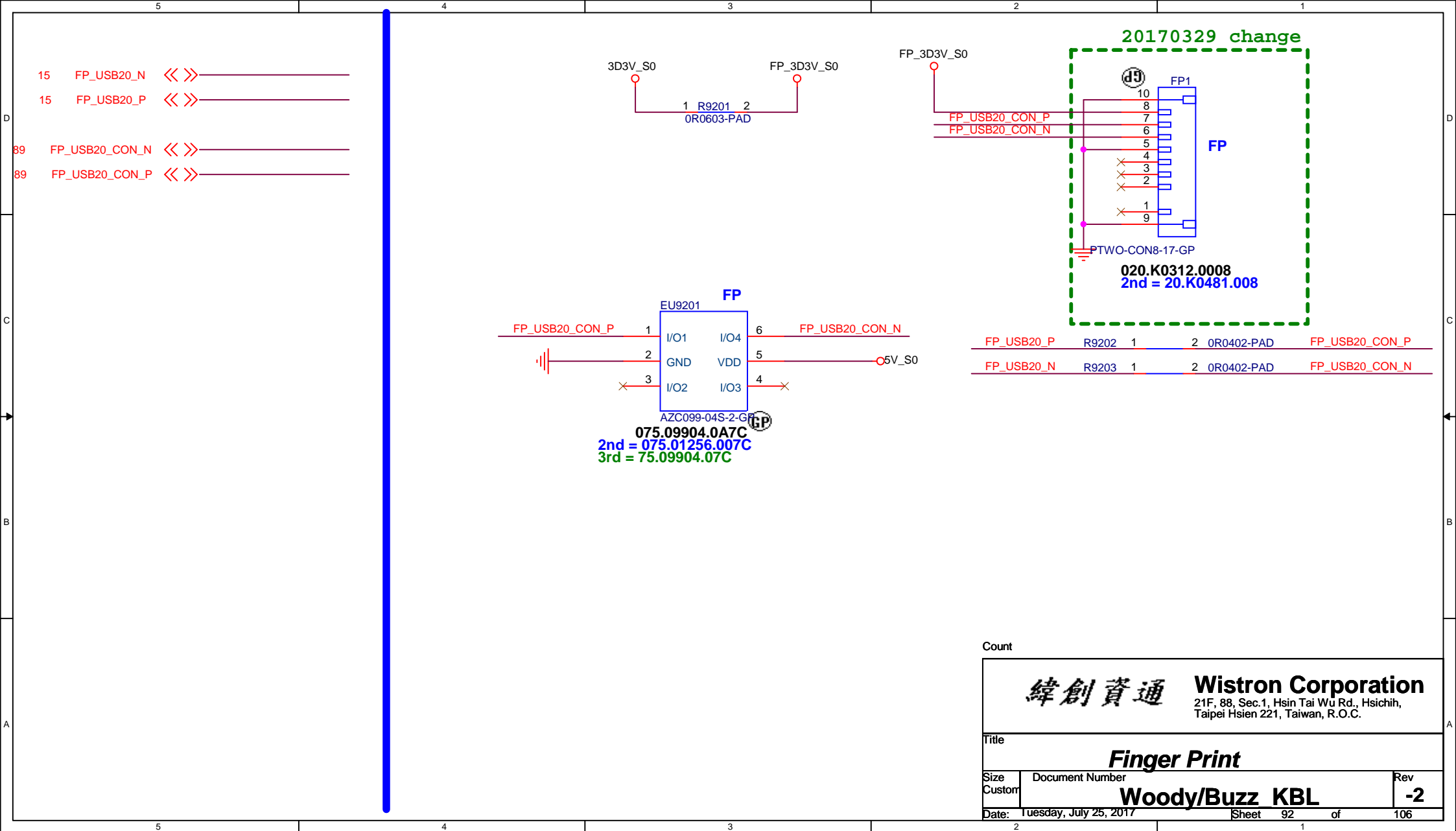
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Rev  
**-2**

Date: Tuesday, July 25, 2017

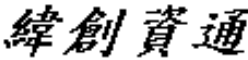
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Title <b><i>Express_Card(Reserved)</i></b>			
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Title <b>Smart Card socket(Reserved)</b>			
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Title			
GFX eDP(Reserved)			
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Title

***Bottom Docking(Reserved)***

Size

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		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>Inter LAN WG1217LM(Reservrd)</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>Woody/Buzz_KBL</div>		<div>Rev</div> <div>-2</div>
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CPU_CFG STRAP(Reserved)</b>			
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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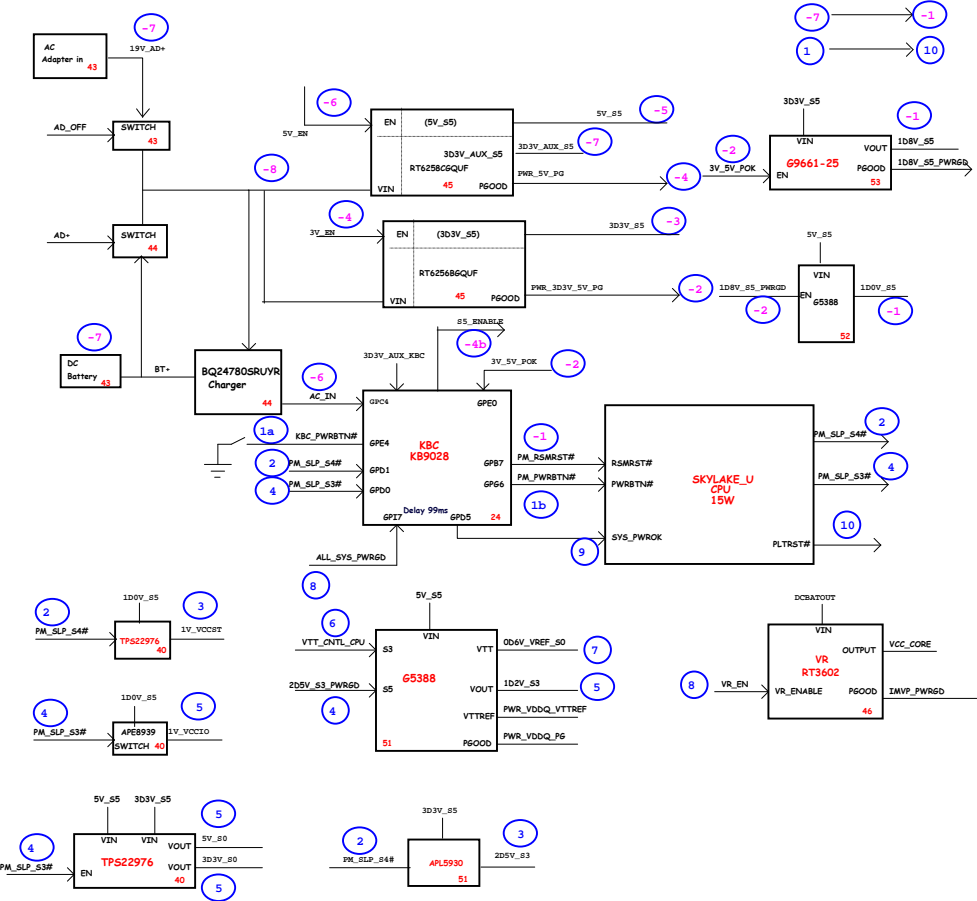
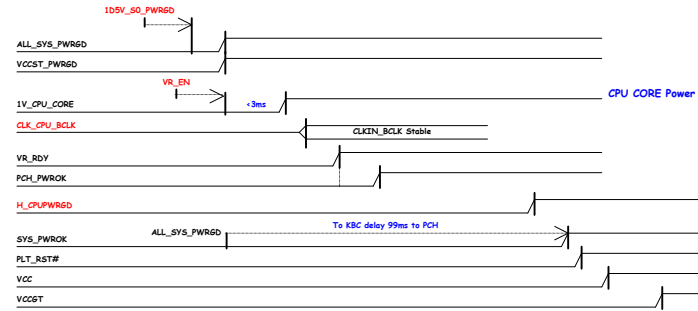
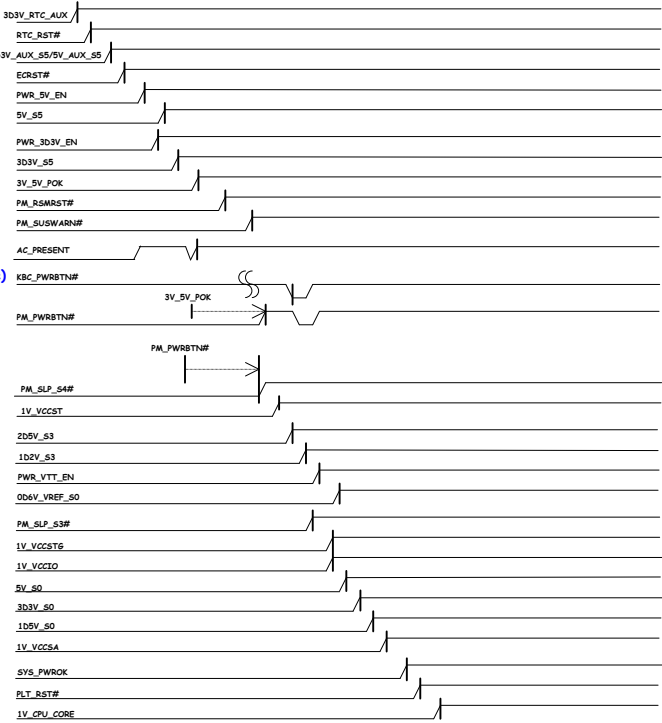
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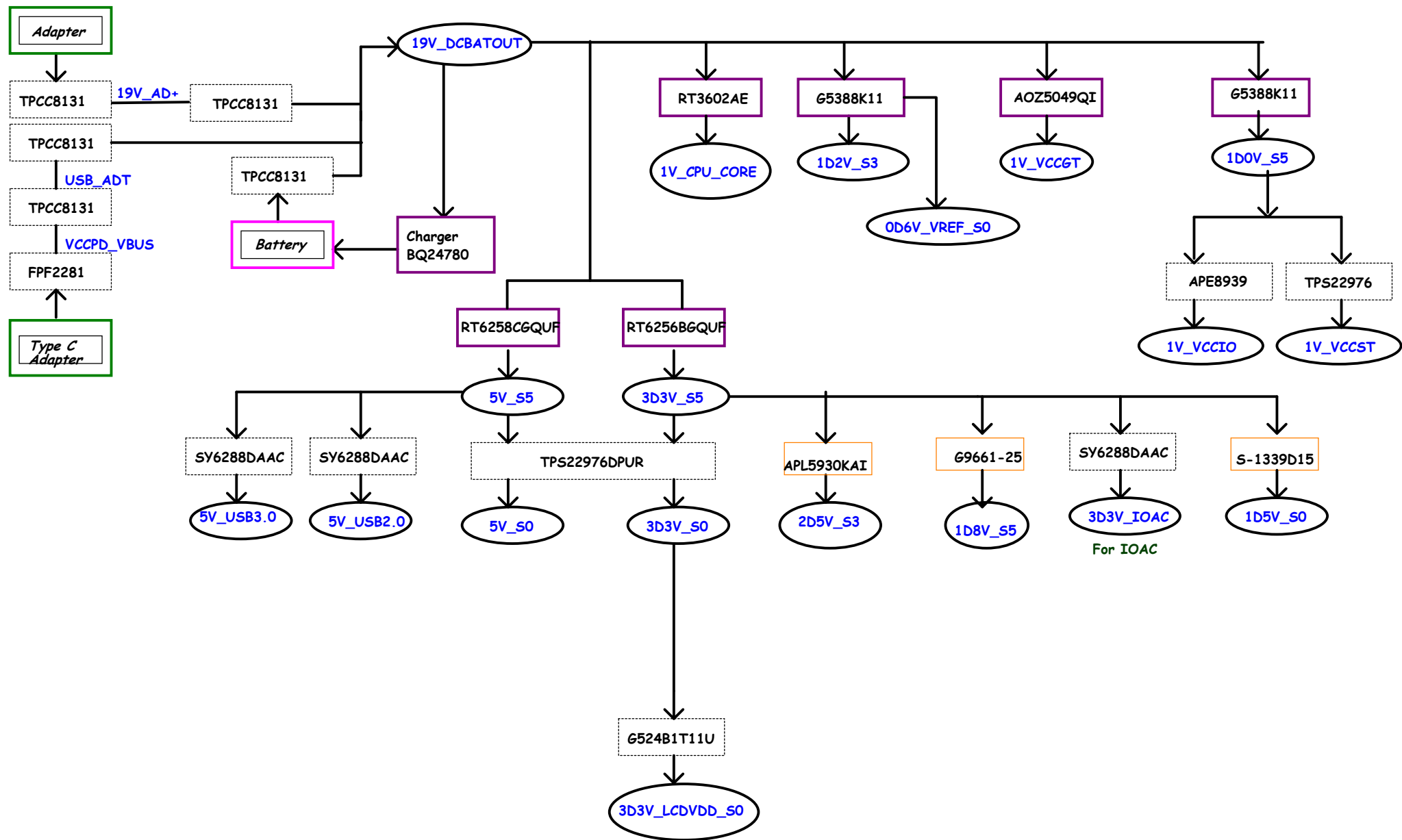


Intel-Power Up Sequence

(AC mode)

(AC mode) (DC mode)





# Power Shape

Regulator

LDO

Switch

Count

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Power Block Diagram**

Size A3 Document Number

**Woody/Buzz\_KBL**

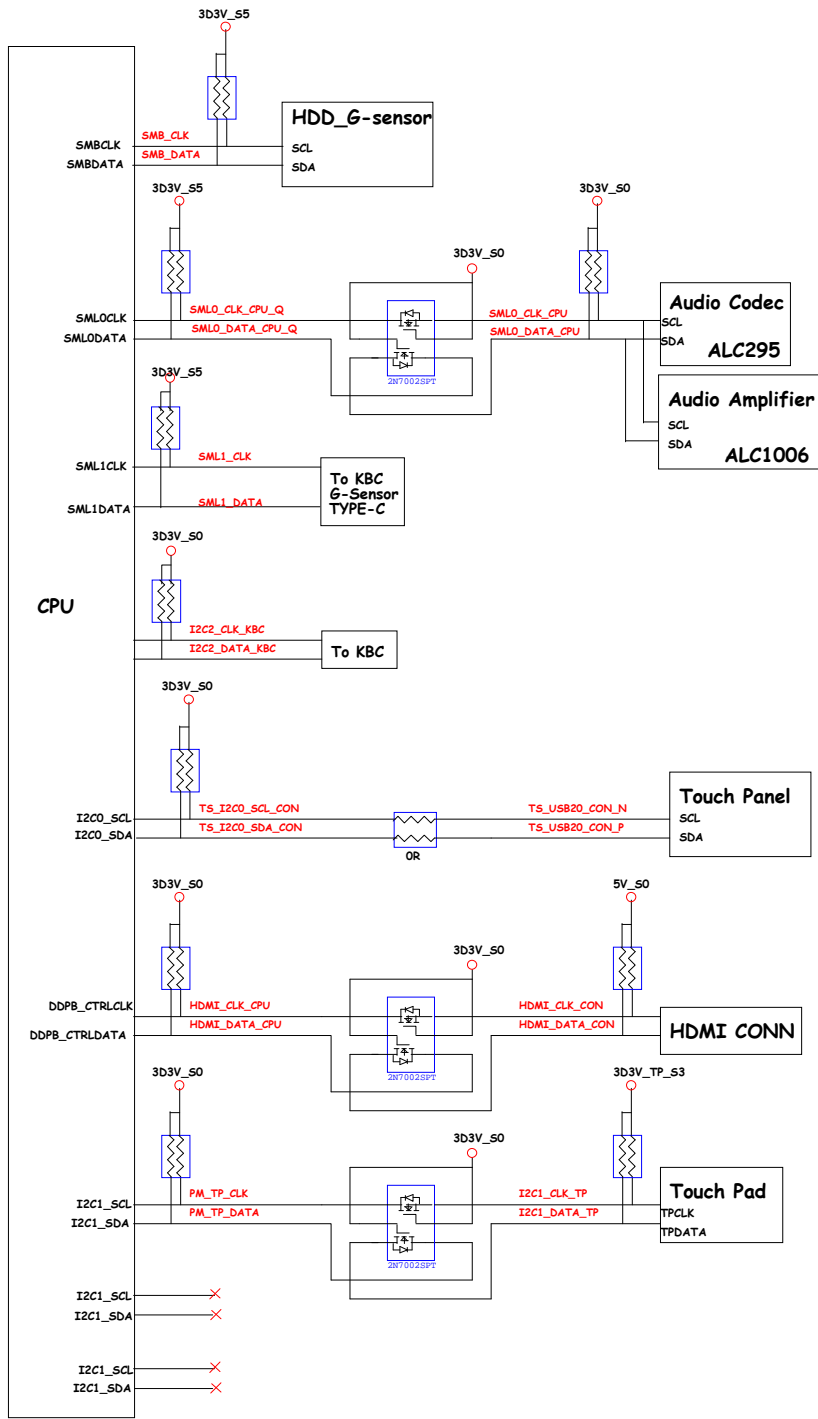
Rev

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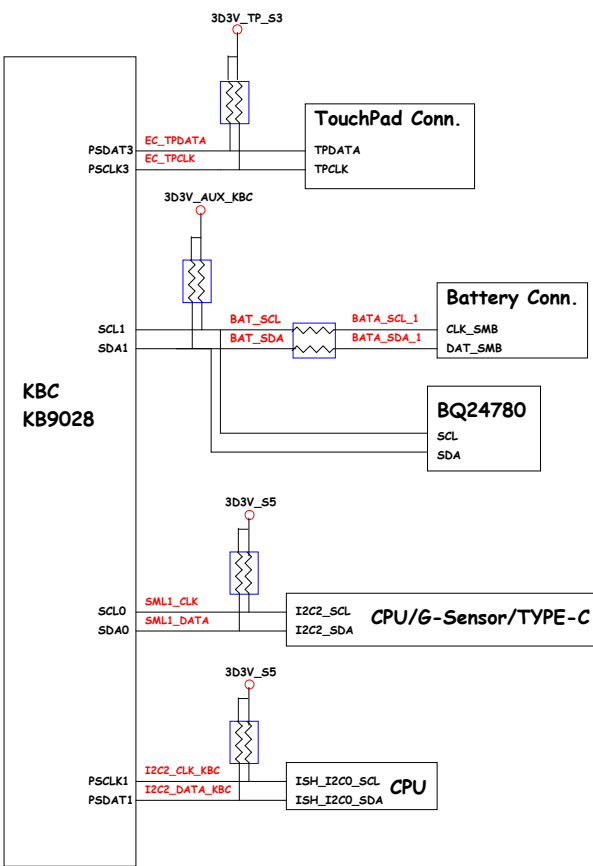
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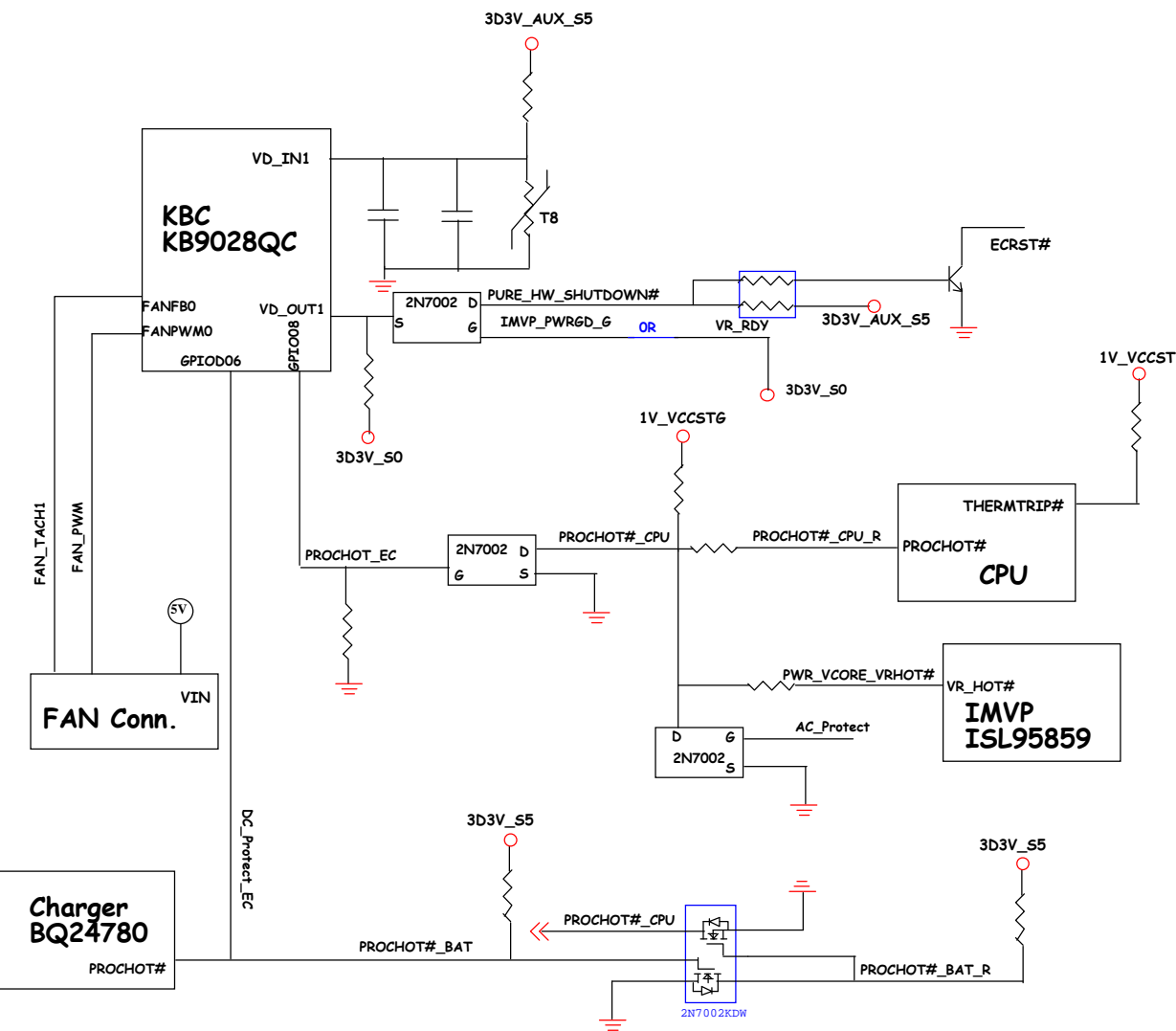
PCH SMBus/I2C Block Diagram



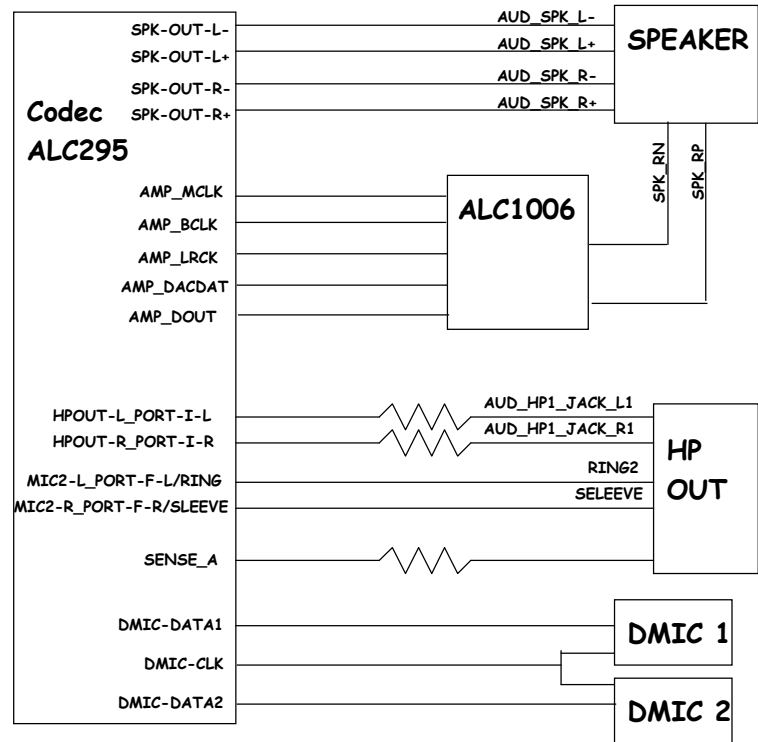
KBC SMBus/I2C Block Diagram



Thermal Block Diagram



Audio Block Diagram





# CLOCK BLOCK DIAGRAM

